SERVICE MANUAL

SERVICE MANUAL

2-B-42

SERVICE MANUAL

1802 / 1820 / 1850 FREQUENCY COUNTER

(B&K)

DYNASCAN CORPORATION
2815 WEST IRVING PARK ROAD
CHICAGO, ILLINOIS 60618

B+K PRECISION

MODEL 1802, 1820 & 1850 FREQUENCY COUNTERS

SERVICE MANUAL

494-059-9-001 B

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ADDITIONAL INFORMATION

MODEL 1802

Instruction Manual 480-219-9-001
Composite 499-123-9-001

MODEL 1820

Instruction Manual 480-216-9-001
Composite 499-122-9-001

MODEL 1850

Instruction Manual 480-218-9-001
Composite 499-128-9-001

INPUT SECTION (Fig. 1A and Fig. 2)

The input section is a wide band amplifier circuit with input protection, X10 attenuation (Models 1820 & 1850), and Schmitt trigger circuitry. The FET, Q1, provides good input sensitivity over the frequency range of 5Hz to 80MHz, and the triple line receiver, IC4, forms a Schmitt tirgger and amplifier.

R10 is a damping resistor that helps filter out any high frequency noise present on low frequency signals. The larger value, 180 Ω, for Models 1802 and 1850, provides better damping, but limits the high frequency sensitivity (50mV RMS at 60MHz). The Model 1820 uses an 82Ω resistor for R10, which allows greater sensitivity (50mV RMS at 80MHz), but has less damping when reading low frequency signals. R7 and D8 and D10 provide a DC path to ground for DC-blocking capacitor C10. R8 provides AC signal protection by limiting the amount of current flow through D8 and D10. C9 is a high frequency by-pass capacitor. D8 and D10 limit the maximum gate signal to plus and minus .7 volts on Q1. R4 provides additional damping of the input signal into Q1. R9 and R11, along with I_{DSS} of the FET, bias Q3 such that the collector is approximately 3 volts. Clamping diode, D9, places the source of Q1 at .7 volts lower than the collector of Q3. R14 and R15 form a voltage divider for X1 and X10 attenuation (Models 1820 and 1850 -- Fig. 1A). Q2 and Q4 turn on alternately by the current flow through either D12, R12 or D13, R13 and effectively couple the signal from the voltage dividers (R14, R15) to "bipolar" capacitor consisting of C12 and C16. The X1/X10 switch applies +10 to D12, R12 (turns Q2 on) and ground to D13, R13 (Q4 off) in the "X10" mode. In the "X1" mode, the voltages are reversed and Q2 is off and Q4 is turned on. The X1 or X10 signal is then applied to the input of the triple line receiver, IC4. Precision resistors, R16, 17, 18, and 19, bias IC4 such that the sensitivity is approximately 30mV RMS of the emitter coupled logic (ECL) device. C13 and C31 are AC signal paths to ground. IC4 is a dual rail

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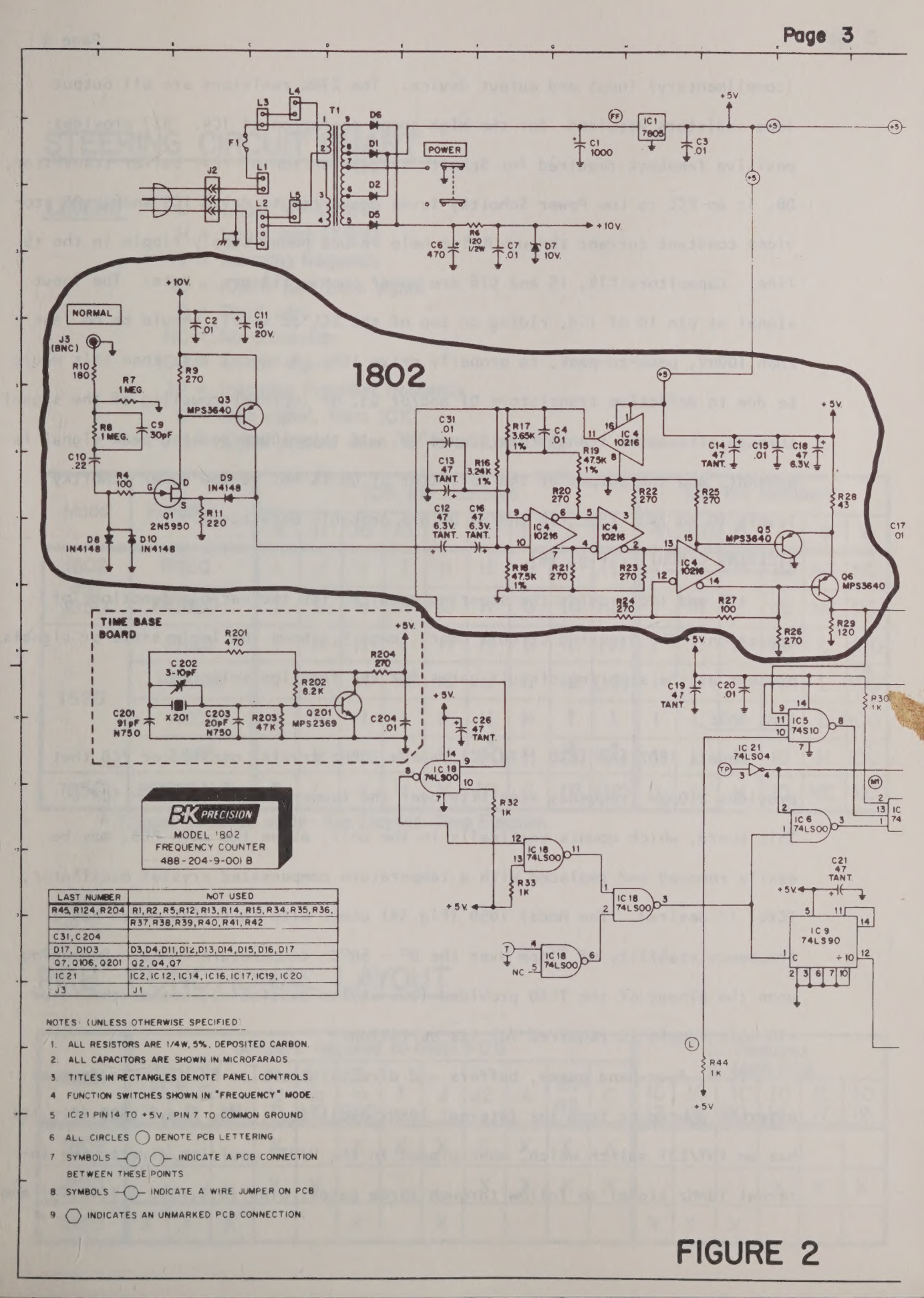


LAST NUMBER	NOT USED
R45, R124, R204	R1, R2, R5, R12, R13, R14, R15, R34, R35, R36, R37, R38, R39, R40, R41, R42
C31, C204	
D17, D103	D3, D4, D11, D12, D13, D14, D15, D16, D17
Q7, Q106, Q201	Q2, Q4, Q7
IC 21	IC2, IC 12, IC14, IC16, IC17, IC19, IC 20
J3	J1

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4W, 5%, DEPOSITED CARBON.
2. ALL CAPACITORS ARE SHOWN IN MICROFARADS.
3. TITLES IN RECTANGLES DENOTE PANEL CONTROLS.
4. FUNCTION SWITCHES SHOWN IN "FREQUENCY" MODE.
5. IC 21 PIN 14 TO +5V., PIN 7 TO COMMON GROUND.
6. ALL CIRCLES ◯ DENOTE PCB LETTERING.
7. SYMBOLS —◯ ◯— INDICATE A PCB CONNECTION BETWEEN THESE POINTS.
8. SYMBOLS —◯— INDICATE A WIRE JUMPER ON PCB.
9. ⬡ INDICATES AN UNMARKED PCB CONNECTION.

FIGURE 2

(complimentary) input and output device. The 270Ω resistors are all output load resistors required for the high speed operation of IC4. R27 provides positive feedback required for Schmitt trigger action of IC4. Buffer transistor, Q6, is an ECL to Low Power Schottky level converter to drive IC5 and6. Q5 provides constant current through R28 to help reduce power supply ripple in the +5 line. Capacitors C14, 15 and C18 are power supply filters. Note: The input signal at pin 10 of IC4, riding on top of the ECL dc level, should be no less than 100mV, peak-to-peak, to properly drive IC4. A signal less than this would be due to defective transistors Q1 and/or Q3, or improper coupling of the signal through attenuator transistors Q2 and Q4. If this 100mV peak-to-peak signal is present, and the output of the collector of Q6 is not at low power Schottky levels (0 to 2V), then IC4 and/or Q6 are probably defective.

STEERING CIRCUIT (Fig. 1B)

IC5 and IC6 provide the steering required for the various functions of operation. The Steering Circuit Chart, page 5, shows the logic state or signals present at the steering circuit gates for the function selected.

TIME BASE

Models 1802 and 1820 (Fig.1C) have a 10MHz crystal oscillator PCB that provides ±10ppm frequency stability over the temperature range 0° - 50° C. This board, which mounts vertically in the unit, above the main PCB, may be easily removed and replaced with a temperature compensated crystal oscillator, TCXO, if desired. The Model 1850 (Fig.3A) comes with this TCXO which has a frequency stability of ±1ppm over the 0° - 50°C temperature range. Depending upon the pinout of the TCXO provided (two styles available), either the +5 or +10 volt supply is required for its operation.

IC18, four nand gates, buffers and directs the time base either from an external source or from the internal 10MHz oscillator. The Model 1820 (Fig.1C) has an INT/EXT switch which, when placed in the "INT" position, directs the internal 10MHz signal to follow through three gates, pins (8,9,10), (11,12,13) and

STEERING CIRCUIT CHART

LEGEND

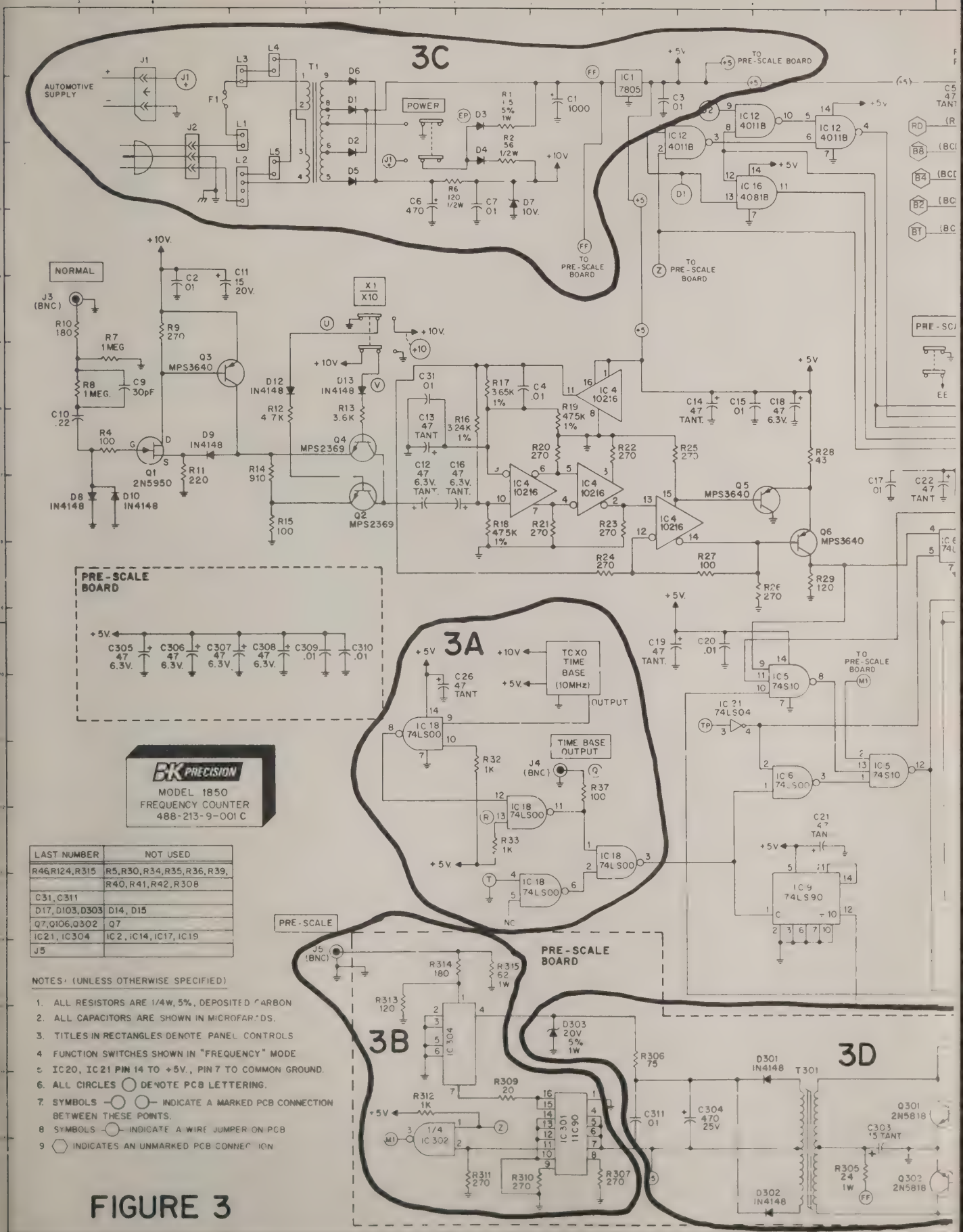
L = Logic low (< .8V)
H = Logic high (> 2V)
I = Incoming frequency
10 = 10MHz time base signal
D = Don't care
NC = No connection
100 = 100Hz signal
IP = Incoming Prescaler frequency
G = Gate signal, from IC10.
( ) = Signal present when "G" is at Logic High

Model	Function	IC5 Pin Numbers									IC6 Pin Numbers					
		9	11	10	13	1	2	3,4	5	6	4	2,5	6	1	9	10
1802 and 1850	FREQ	I	H	H	I	H	H	G	I	(I)	I	L	H	10	NC	NC
	PERIOD	I	L	H	H	10	H	G	10	(10)	I	H	I	10	NC	NC
1820	FREQ	I	H	H	I	H	H	G	I	(I)	I	L	H	10	L	100*
	PERIOD	I	L	H	H	10	H	G	10	(10)	I	H	I	10	L	100*
	ACCU	I	H	H	I	H	H	H	I	I	I	L	H	10	L	100*
	TIME	I	H	L	H	H	100*	H	100*	100*	I	L	H	10	H	100*
1850	PRESCALE	D	L	H	H	H	IP	G	IP	(IP)	D	L	H	10	NC	NC

* Trigger in active state - See Elapsed Time Function.

PCB FUNCTIONAL LAYOUT

Model	Jumpers required on Main PCB												IC Required in Main PCB					
	Prescale PCB to			N to P	M1 to M2	T to GRD	I	J	J2	A	B1 B2	C	IC 12	IC 16	IC 20	IC 14	IC 17	IC 19
	N	P	M1															
1802				X		X	X	X	X	X	X	X						
1820				X	X				X	X	X	X				X	X	X
1850	X	X	X			X		X					X	X	X			

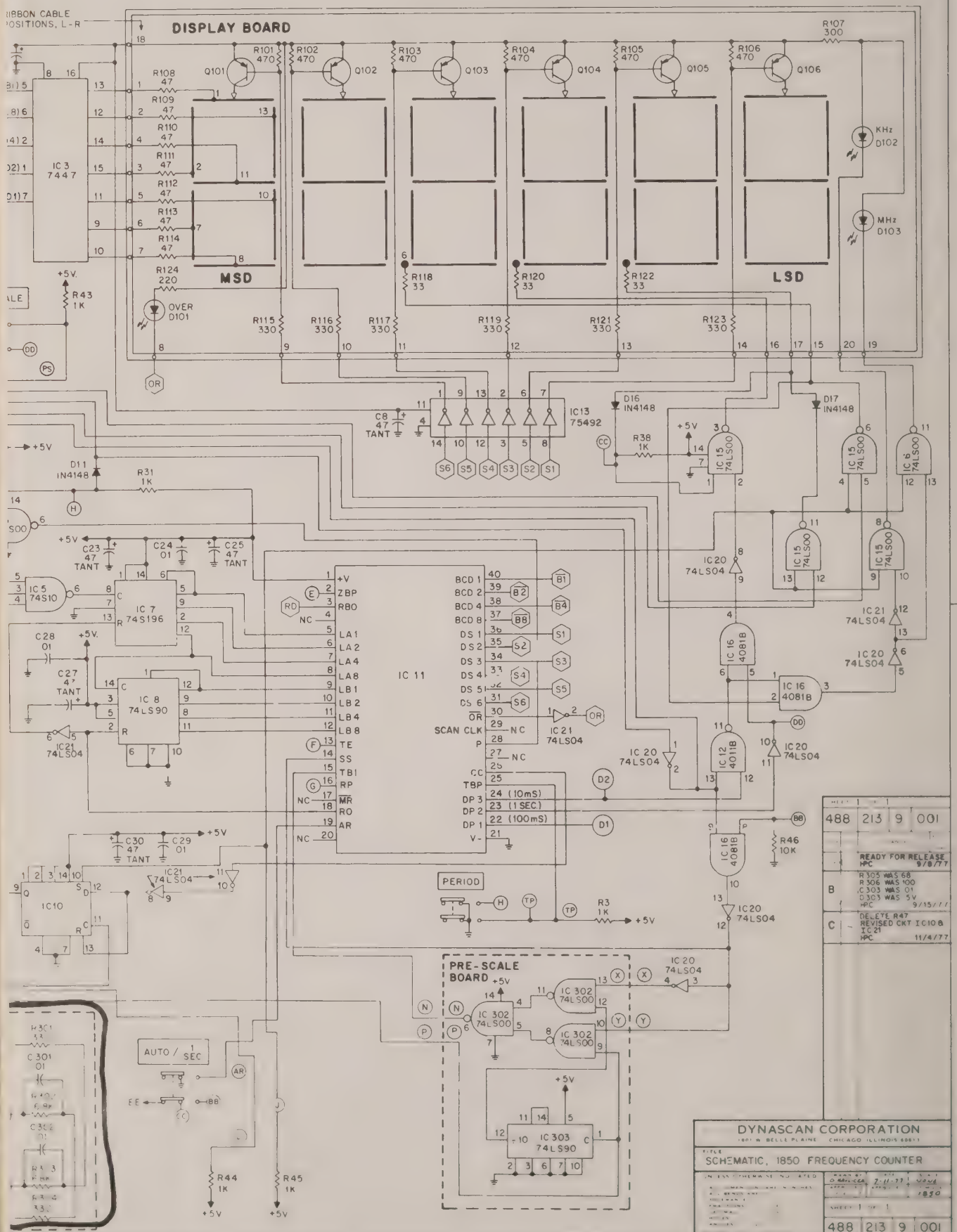


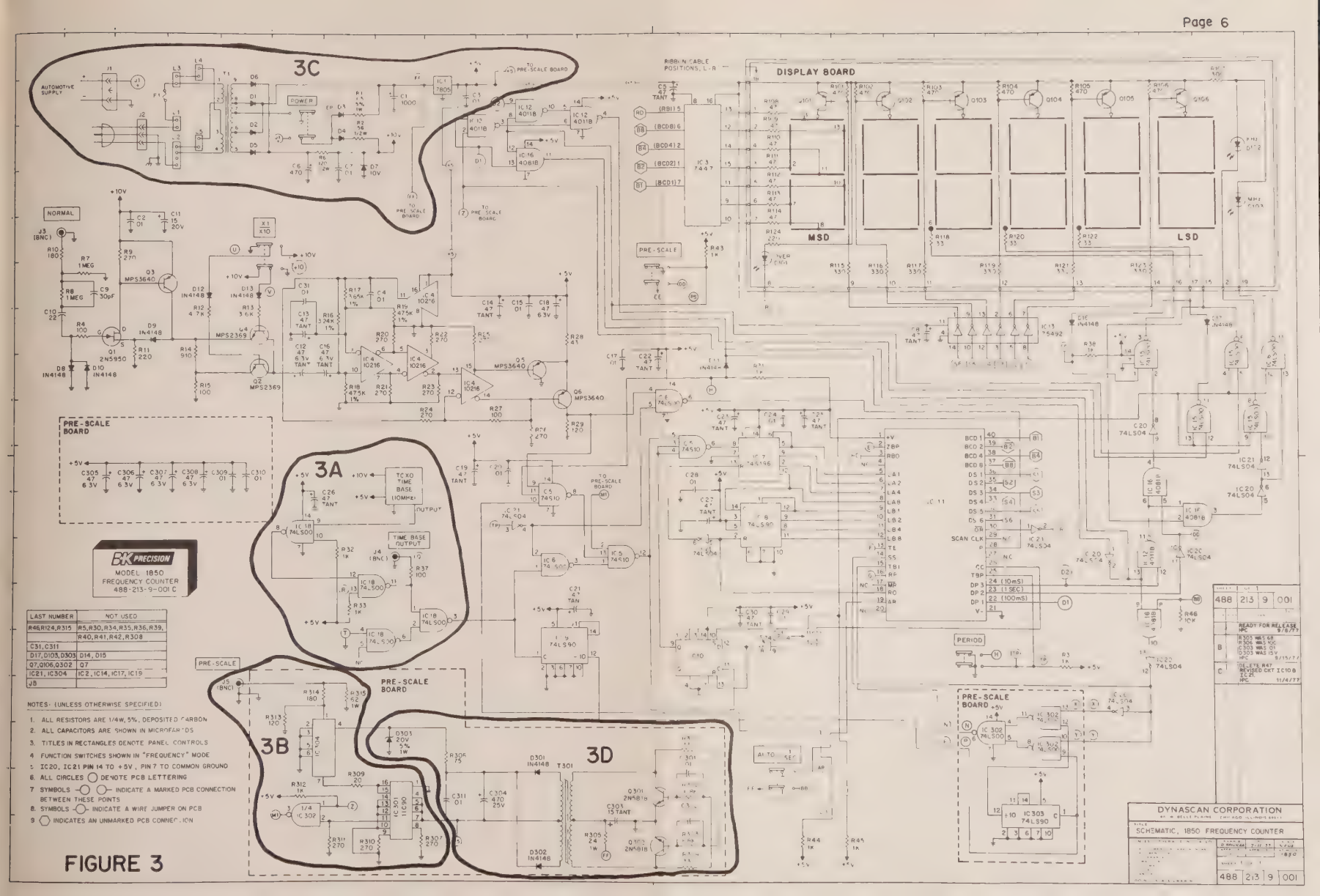
LAST NUMBER	NOT USED
R46,R124,R315	R5,R30,R34,R35,R36,R39,
	R40,R41,R42,R308
C31,C311	
D17,D103,D303	D14, D15
Q7,Q106,Q302	Q7
IC21, IC304	IC2, IC14, IC17, IC19
J5	

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4W, 5%, DEPOSITED CARBON
2. ALL CAPACITORS ARE SHOWN IN MICROFARADS.
3. TITLES IN RECTANGLES DENOTE PANEL CONTROLS
4. FUNCTION SWITCHES SHOWN IN "FREQUENCY" MODE
5. IC20, IC21 PIN 14 TO +5V., PIN 7 TO COMMON GROUND.
6. ALL CIRCLES ◯ DENOTE PCB LETTERING.
7. SYMBOLS —◯ ◯— INDICATE A MARKED PCB CONNECTION BETWEEN THESE POINTS.
8. SYMBOLS —◯— INDICATE A WIRE JUMPER ON PCB
9. ⬡ INDICATES AN UNMARKED PCB CONNECTION

FIGURE 3


DISPLAY BOARD
MSD
LSD
IC 3 7447
IC 11
IC 13 75492
IC 7 74S196
IC 8 74LS90
IC 10
IC 302 74LS00
IC 303 74LS90
PRE-SCALE BOARD +5V
PERIOD
AUTO / 1 SEC
OVER D101
KHz D102
MHz D103
SCAN CLK
DYNASCAN CORPORATION
SCHEMATIC, 1850 FREQUENCY COUNTER
488 213 9 001
READY FOR RELEASE HPC 9/8/77
R305 WAS 68
R306 WAS 100
C303 WAS 01
D303 WAS 5V
HPC 9/15/77
DELETE R47
REVISED CKT IC10B
IC21
HPC 11/4/77



LAST NUMBER	NOT USED
R46,R124,R315	R5,R30,R34,R35,R36,R39, R40,R41,R42,R308
C31, C311	
D17,D103,D303	D14, D15
Q7,Q106,Q302	Q7
IC21, IC304	IC2, IC14, IC17, IC19
J8	

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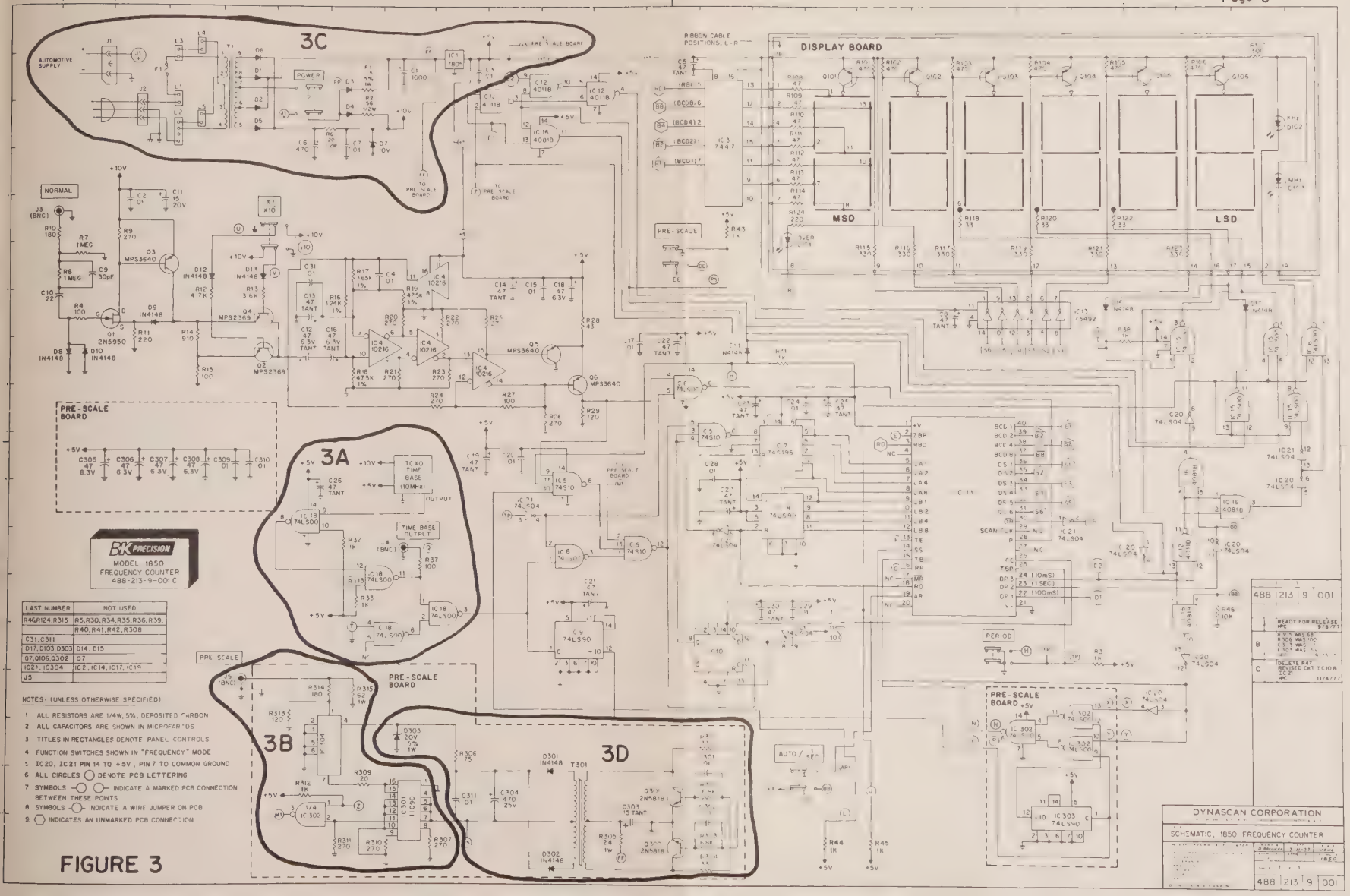
3. TITLES IN RECTANGLES DENOTE PANEL CONTROLS
4. FUNCTION SWITCHES SHOWN IN "FREQUENCY" MODE
5. IC20, IC21 PIN 14 TO +5V, PIN 7 TO COMMON GROUND
6. ALL CIRCLES ◯ DENOTE PCB LETTERING
7. SYMBOLS —◯— ◯— INDICATE A MARKED PCB CONNECTION BETWEEN THESE POINTS
8. SYMBOLS —◯— INDICATE A WIRE JUMPER ON PCB
9. ◯ INDICATES AN UNMARKED PCB CONNECTION

B	R303 WAS 68K R306 WAS 90 C303 WAS 01 D303 WAS 15V HPC		8/15/77
C	DELETE R47 REVISED CKT IC10 & IC21 HPC		11/4/77

FIGURE 3



LAST NUMBER	NOT USED
R46,R124,R315	R5,R30,R34,R35,R36,R39, R40,R41,R42,R308
C31, C311	
D17, D103, D303	D14, D15
Q7,Q106,Q302	Q7
IC21, IC304	IC2, IC14, IC17, IC19
J5	

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4W, 5%, DEPOSITED CARBON
2. ALL CAPACITORS ARE SHOWN IN MICROFARADS
3. TITLES IN RECTANGLES DENOTE PANEL CONTROLS
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5. IC20, IC21 PIN 14 TO +5V, PIN 7 TO COMMON GROUND
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8. SYMBOLS —◯ INDICATE A WIRE JUMPER ON PCB
9. ◯ INDICATES AN UNMARKED PCB CONNECTION

FIGURE 3

(1,2,3) of IC18, and on to drive IC's 9, 10, and 21. In the "EXT" position, an external 10MHz TTL compatible signal, entered through the "EXTERNAL TIMEBASE" rear jack, is directed through two gates, pins (4,5,6) and (1,2,3) of IC18, to drive IC's 9, 10, and 21. Gate (11,12,13) is disabled, cutting off the internal 10MHz timebase. R40 and D15 protect the external timebase input by allowing up to 7 volts "high" level from the source signal without damaging the input circuitry. Model 1802 has pin 13 pulled to +5 through R33 and pin 4 hard-wired ("T" jumper) to ground so that no external input can be entered. However, the Model 1802 can be modified by adding the INT/EXT switch, BNC jack, and R40 and D15 to accept an external time base. The Model 1850 (Fig. 3) also has pin 13 tied to +5 and pin 4 connected to ground, but has an output signal available from the internal TCXO. Buffered by gates, pins (8,9,10) and 11,12,13) of IC18, this 10MHz output is connected to the BNC jack through R37, which protects the output from short circuit damage.

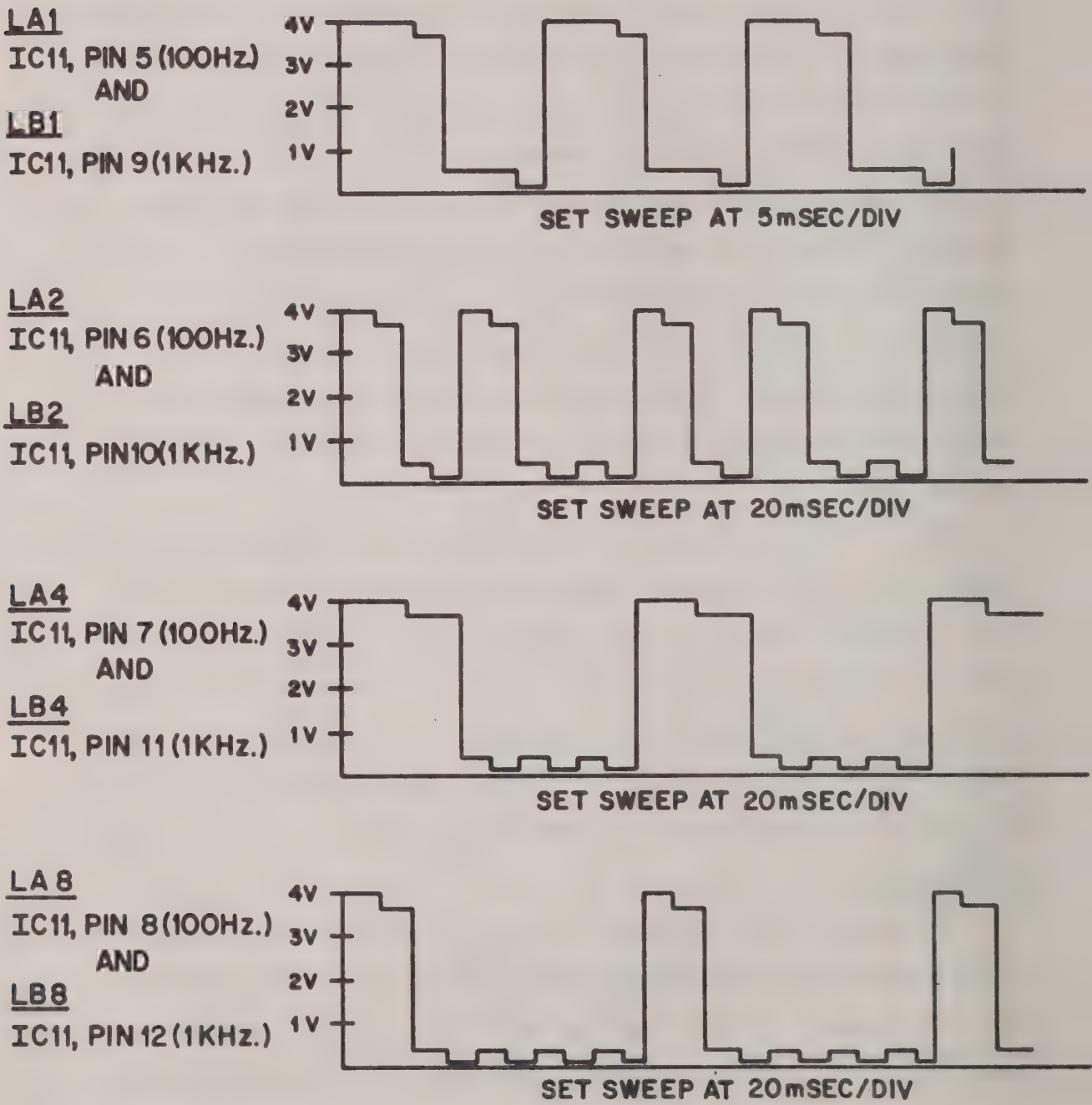
IC9, divide-by-ten counter, provides the 1MHz signal required for the LSI counter chip, IC11, to operate. This signal comes either directly from the output of IC9, pin 12, in the Models 1802 and 1820,or through the prescale board in the Model 1850. The prescale board provides a divide-by-1 (1MHz) or divide-by-10 (100KHz) signal. Only in the PRESCALE mode, when the 1 SEC push-button is "in", does the divide-by-10 (100KHz) signal become active to allow a 10 second gate interval to occur. See Prescale Function.

COUNTER SECTION (Fig. 1D)

The counter circuitry consists of IC7, IC8, IC10 and IC11. IC7 and IC8 are divide-by-ten counters that produce a BCD coded output into IC11 (See Fig. 4). IC11, the custom L.S.I. chip, contains all the counting logic required for the function selected. IC11 is driven by a 1MHz time base and internally develops the strobe pulses, DS1 through DS6 (see Display Section), the count control (CC), reset out (RO) (see Frequency Function) and decimal point select (DP1, 2 and 3)

NOTES:

(1) WAVEFORMS LA1, 2, 4 AND 8 WITH INPUT SIGNAL AT 100Hz.
(2) WAVEFORMS LB1, 2, 4 AND 8 WITH INPUT SIGNAL AT 1KHz.
(3) WAVEFORMS PRESENT ONLY WHEN COUNT CONTROL (CC) IS HIGH; WHEN CC IS LOW, STATE IS EITHER HIGH OR LOW.



COUNTER SECTION
FIG. 4

necessary for the counting and display functions. One-half of device IC10, the dual "D" flip-flop, pins 1-7 is not used. The other "D" flip-flop, pins 9 - 13 of IC10, speeds up the count control rise and fall time and synchronizes the rising edge of the CC with the incoming signal in order to insure proper registering of the first full cycle of the incoming signal. This prevents the frequency from being displayed one-half of a count too high and disturbing the frequency-period reciprocal factor.

FREQUENCY FUNCTION (Fig. 5)

Selection of the frequency mode of operation, depressing the FREQ. push-button, mechanically releases the other FUNCTION switch(es) to the "OUT" position. No electrical switch is located behind the FREQ. button - an interlock is present to release the other FUNCTION switch(es). The charts of the Steering Circuit (page 5) and the Display Logic (page 23, see Display Section) illustrate the logic states present for the Frequency Function. Depending upon the input frequency being counted "CC" (count control) will go "high" for three different time period intervals. These are as follows (AUTO/1 SEC switch in the "AUTO" position): Incoming frequency less the 1MHz, CC = 1 sec. (high); incoming frequency greater than 1MHz but less than 10MHz, CC = 100msec (high); and for incoming frequency greater than 10MHz, CC = 10msec (high). See waveforms, Fig. 6. Note that CC must remain low for a minimum of about 200msec in each of the three CC time period intervals. This is due to and internal hold-off delay timing in IC11 to eliminate flickering of the display reading in the 100msec and 10msec CC modes. Pin 24 output of IC11 goes high only during the CC = 10msec mode, turning on the appropriate decimal point (see Display Section). Likewise, pin 22 goes high during the CC = 100msec mode and pin 23 goes high only during the CC = 1 sec. mode. Therefore, only one decimal point can be on at any one time.

FREQUENCY FUNCTION
BLOCK DIAGRAM

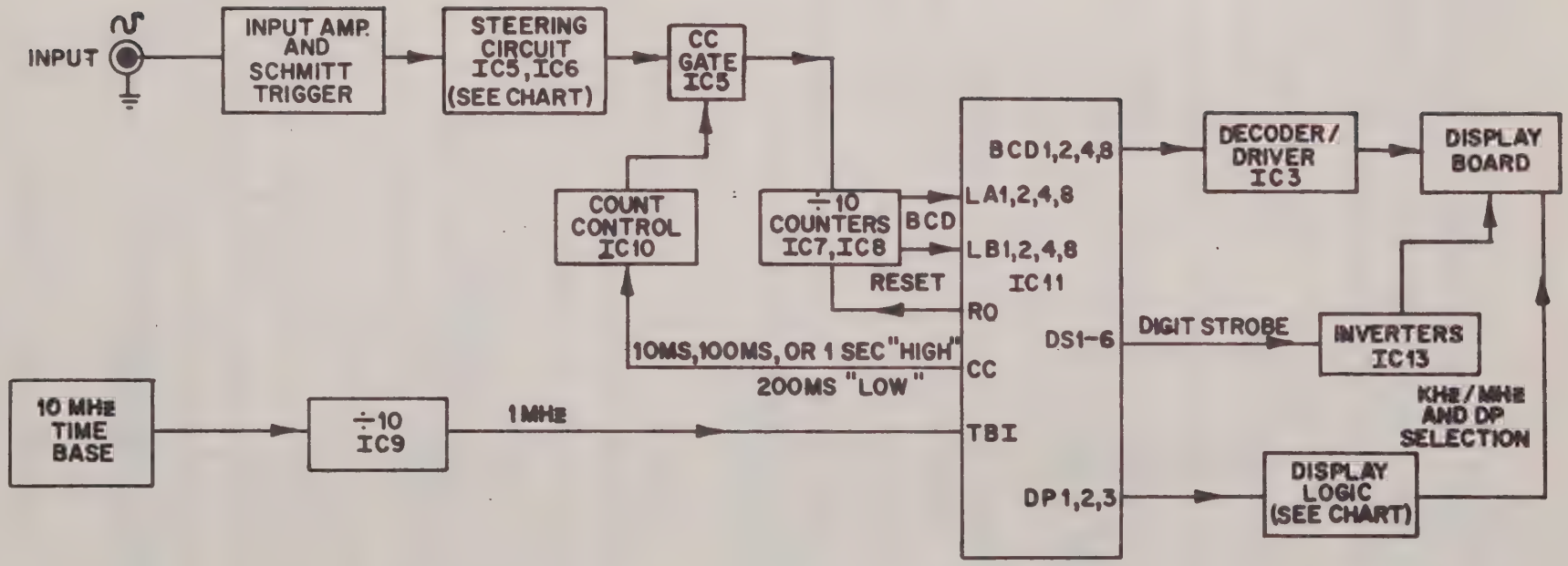
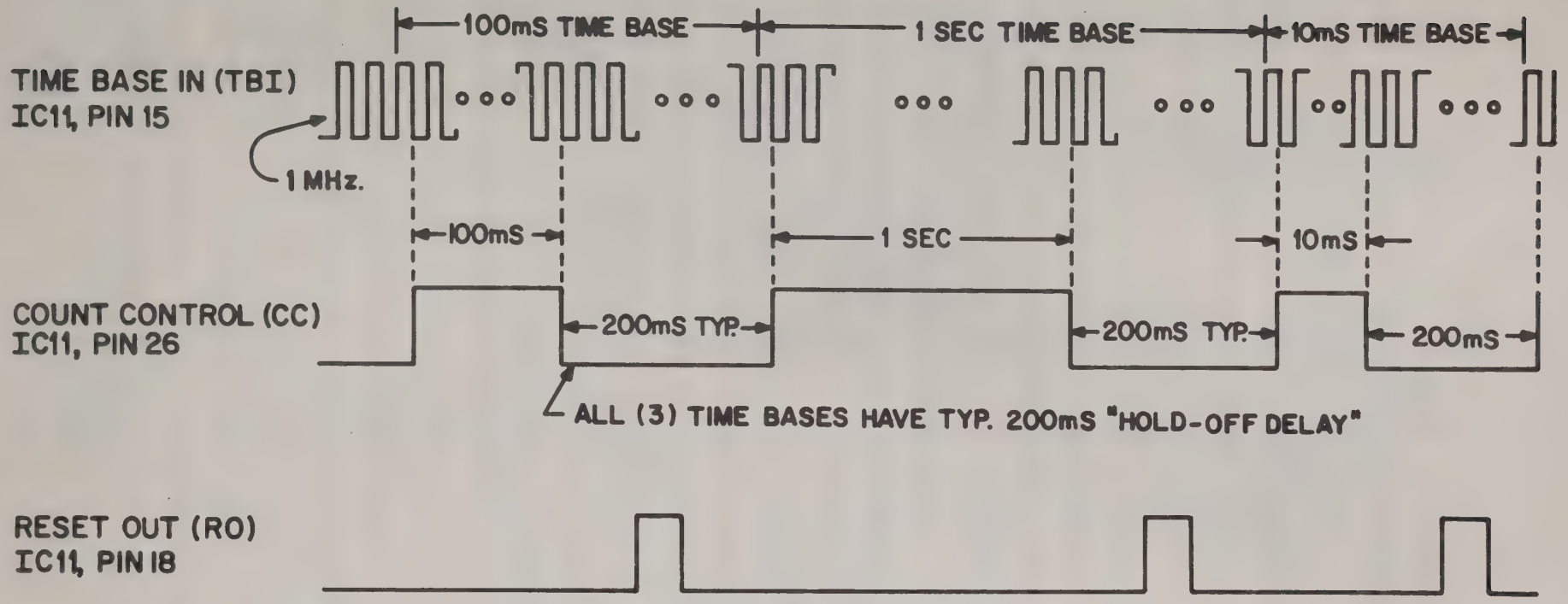


FIG. 5

NOTE:

THREE SEPARATE TIME BASES GENERATED BY IC11 DEPENDING UPON INCOMING FREQUENCY (AUTO. SW. POS.).



COUNT CONTROL AND RESET OUT

FIG. 6

PERIOD FUNCTION (Fig. 7)

Depressing the PERIOD push-button places the counter in the period mode of operation. Note that the other FUNCTION switch(es) must be in the "OUT" position. Points "H" and "TP" on the main PCB are shorted to ground when the PERIOD switch in "IN". The TBP input (pin 25) of IC11 is grounded by Point "TP". This is the "signal" to the custom L.S.I. chip that it must operate in the period mode. Points "H" and "TP" also switch various gates in the steering circuit to direct the 10MHz timebase into the counter section and the incoming signal to the P input (pin 28) of IC11. See Steering Circuit Chart, page 5. The incoming signal, now at "P", controls the length of the CC (count control) logic "high", which is independent of the 1MHz signal at the "TBI" input. CC has three gate times, depending upon the incoming frequency, of 1, 10, or 100 period average. The steering circuit directs the 10MHz time base signal to the divide-by-ten counters, IC7 and IC8, where the incoming frequency previously was directed (in the FREQ mode of operation). This 10MHz signal passes through IC7 and IC8 only when the CC is at logic high. The Display Logic Chart (see Display Section) gives the display L.E.D. indicators lit for the incoming frequencies specified in the PERIOD mode.

ACCUMULATE FUNCTION (Fig. 8, Model 1820 only)

Depressing the ACCU switch activates the accumulate mode. The accumlate function is similar to the frequency function, except that the count control, CC, is set "high" and therefore the gate time is indefinite (continuous). The display will show the total amount of cycles accumulated during this interval. The display may then be reset at anytime by the front panel RESET. The RESET switch is inactive in the FREQ and PERIOD functions. The RO output (pin 18) of IC11 will only go "high" when the RESET button is pushed. When the ACCU push-button is depressed, four (4) points on the main PCB are brought to ground.

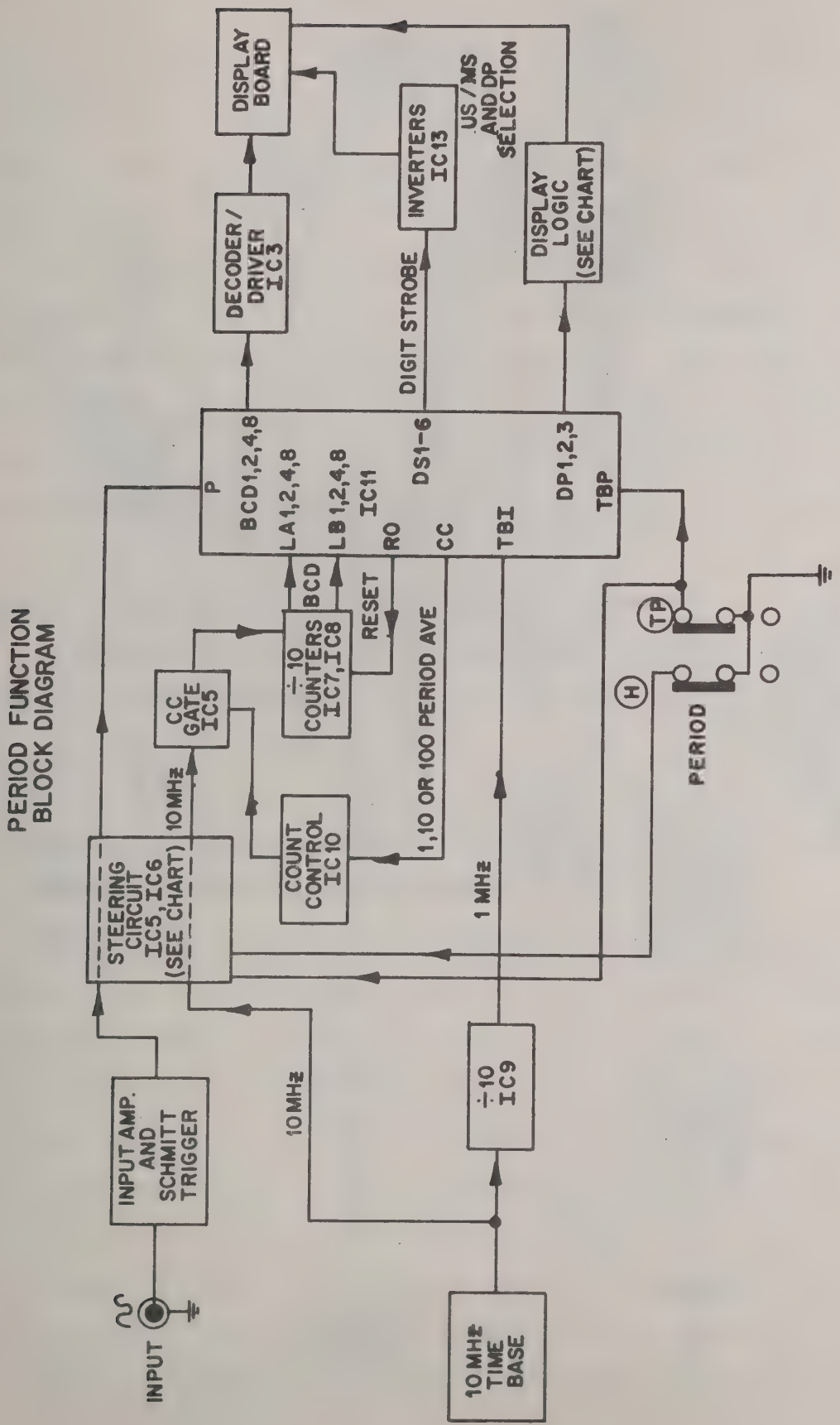

PERIOD FUNCTION
BLOCK DIAGRAM
INPUT
INPUT AMP. AND SCHMITT TRIGGER
STEERING CIRCUIT IC5, IC6 (SEE CHART)
10 MHz
CC GATE IC5
÷10 COUNTERS IC7, IC8
BCD
RESET
COUNT CONTROL IC10
1, 10 OR 100 PERIOD AVE
1 MHz
÷10 IC9
10 MHz
10 MHz TIME BASE
P
BCD1,2,4,8
LA1,2,4,8
LB1,2,4,8
IC11
RO
CC
TBI
DS1-6
DP1,2,3
TBP
DIGIT STROBE
DECODER / DRIVER IC3
DISPLAY BOARD
INVERTERS IC13
US / MS AND DP SELECTION
DISPLAY LOGIC (SEE CHART)
TP
H
PERIOD

FIG. 7

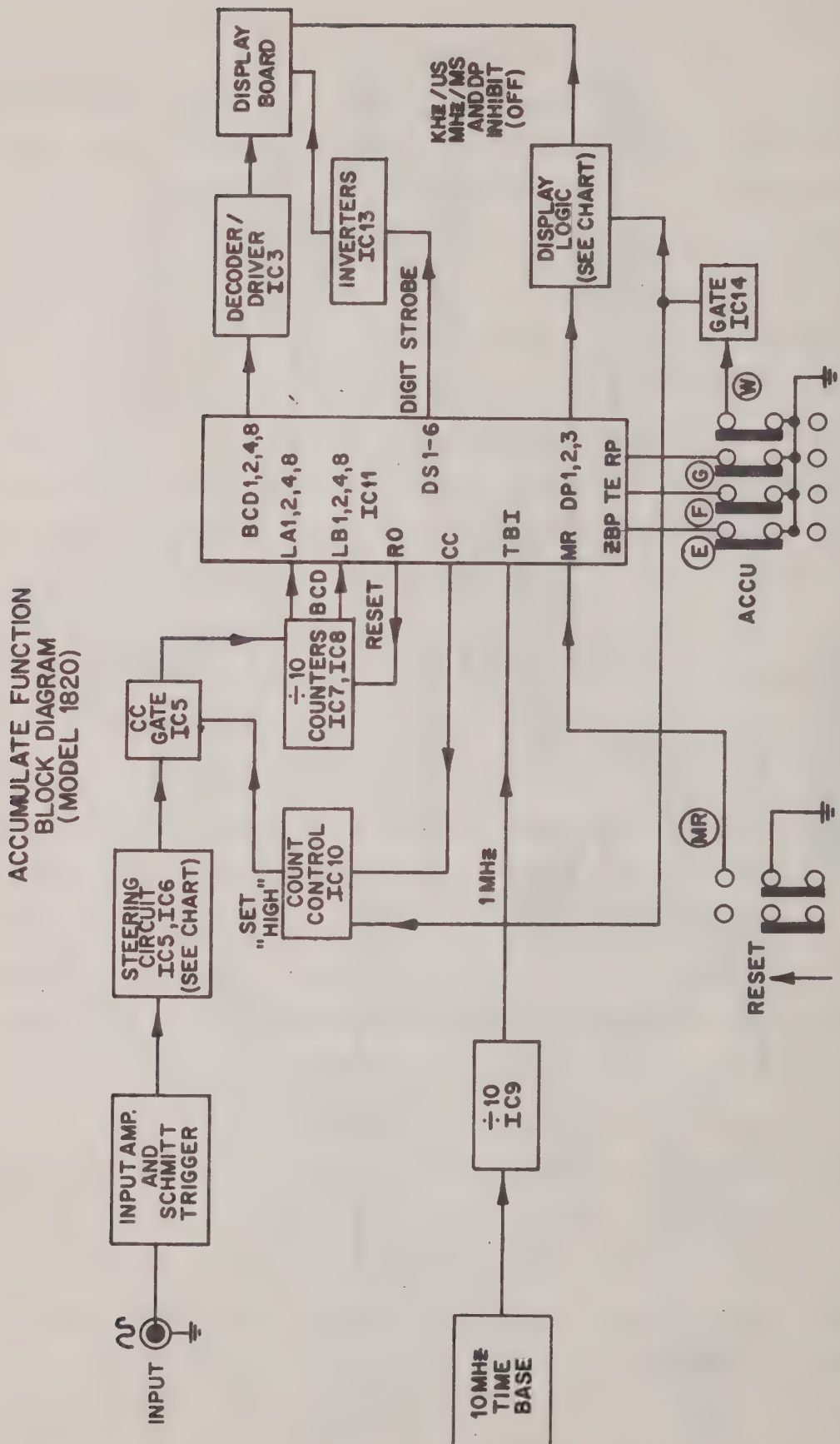

ACCUMULATE FUNCTION
BLOCK DIAGRAM
(MODEL 1820)
INPUT
INPUT AMP. AND SCHMITT TRIGGER
STEERING CIRCUIT IC5, IC6 (SEE CHART)
CC GATE IC5
÷10 COUNTERS IC7, IC8
BCD
RESET
SET "HIGH"
COUNT CONTROL IC10
10 MHz TIME BASE
÷10 IC9
1 MHz
BCD1,2,4,8
LA1,2,4,8
LB1,2,4,8
IC11
RO
DS1-6
CC
TBI
MR
DP1,2,3
ZBP TE RP
DIGIT STROBE
DECODER / DRIVER IC3
INVERTERS IC13
DISPLAY BOARD
KHz/US MHz/MS AND DP INHIBIT (OFF)
DISPLAY LOGIC (SEE CHART)
GATE IC14
ACCU
E
F
G
W
MR
RESET

FIG. 8

These are points "E", "F", "G", and "W". Point "E" pulls the ZBP input (pin 2) of IC11 to ground and causes the display to blank all leading zeros except the least significant zero when the RESET switch is pushed. See Display Section. Point "F" pulls the TE input (pin 13) of IC11 to ground, which makes the six internal latches, corresponding to the numberical displays, transparent to the incoming signal. Thus, the count is displayed and updated in the latches immediately as the signal is accumulated. The RP input (pin 16) of IC11 is pulled to ground by point "G" and this activates the external RESET input, $\overline{MR}$ (pin 17). The CC is set "high" and the decimal points and KHz/us-MHz/ms indicators are turned off (see Display Logic Chart, Page 23) when point "W" is brought to ground in the ACCU mode.

ELAPSED TIME FUNCTION (Fig. 9, Model 1820 only)

The elapsed time function displays time in hundredths of a second and has an external trigger input control and reset. The trigger input signal must be TTL compatible and the interval, or "window", that this signal is "high" determines the elapsed time. The positive going edge of this "window" starts the time count and the negative going edge stops the count. The RESET button must then be pushed to reset the trigger logic circuitry.

When no trigger control signal is applied, a logic high is assumed and the counter will continually display time, but can be reset anytime by the front panel control. When the TIME switch is depressed, points "F", "G", "AR", and "L" are brought to ground. Point "F" pulls the TE input (pin 13) of IC11 to ground which makes the six internal latches transparent, as in the accumulate mode. Also, the RP input (pin 16) of IC11 is grounded by point "G" and this activates the $\overline{MR}$ input (pin 17). AR (pin 19) brought to ground assures that IC11 is in the "1 second" CC mode, which gives proper digit blanking so that only the (3) least significant digits read "0" when the RESET switch is depressed - the (3) most significant digits are blanked. Point "L" switches the steering circuit

ELAPSED TIME FUNCTION
BLOCK DIAGRAM
(MODEL 1820)

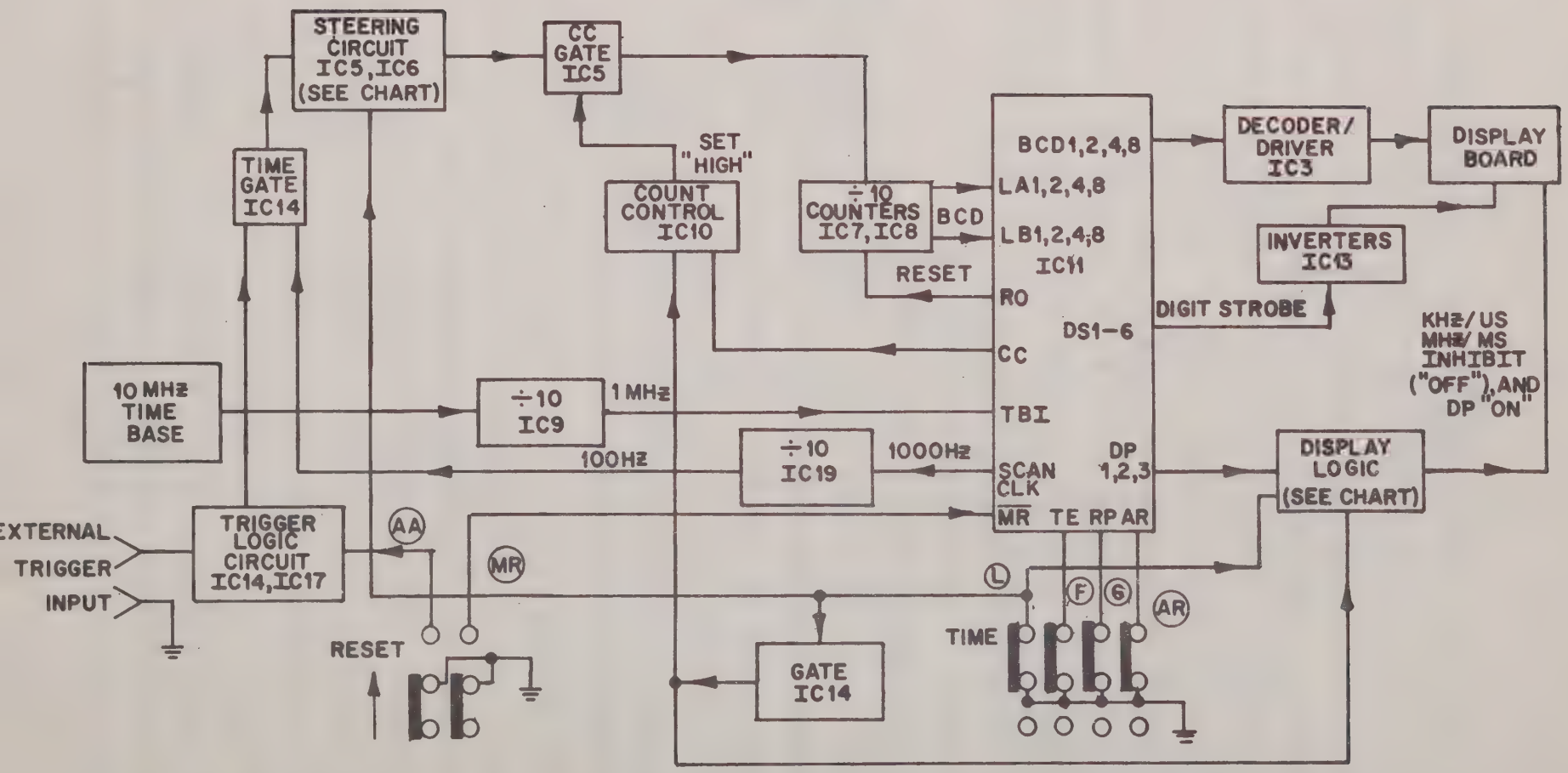


FIG. 9

and the display logic such that the input amplifier is disabled and the 100Hz signal, trigger controlled, is enabled into the counter section and the appropriate decimal point is selected for .01 second resolution. See Steering Circuit (Pg. 5) and Display Logic(Pg.23) charts. Also, the count control output from IC10 is set "high" so that the input into the counters IC7 and IC8 is only dependent upon the 100Hz trigger controlled signal. IC11 internally generates a 1000Hz pulse signal at the SCAN CLK (pin 29) output. This signal is then divided-by-ten at IC 19 and the 100Hz signal is available at pin 13 of IC14 for trigger control. Fig.1E shows the trigger control logic circuitry. When the RESET button is momentarily depressed, point "AA" goes to ground, which initializes the trigger logic flip-flops (IC 17) such that a "high" going signal (or open) at the trigger input starts the time count. Pin 9 of IC14 is initially "high" after reset and pin 8 follows the input signal at pin 10, the trigger input. The Q out of IC17, pin 5, will follow the D input after the first rising edge of the C input, pin 3 (1 MHz). When Q out goes "high", this allows pin 12 of IC14 to go "high" and pass the 100Hz signal at pin 11. When the trigger input goes "low", pin 8 of IC17 goes "low" also, and the Q out, pin 5, of IC17 will go "low" on the next rising edge of the clock input, pin 3. This will stop the 100Hz signal at pin 11 of IC14. Note that as the Q out, pin 5, goes "low", the Q out, pin 6, goes "high", and this makes the Q out, pin 9, go "low" (D input, pin 12, is always "low"), and thus the circuit must now be reset before another trigger input signal will pass through pin 8 of IC14.

PRE-SCALE FUNCTION (Fig. 10, Model 1850 only)

When the PRE-SCALE switch is depressed, the NORMAL input amplifier is disabled and the PRE-SCALE amplifier with divide-by-ten circuit is enabled into the counter section. This happens when point "PS" is pulled to ground. Also, the display logic is "signaled" by point "PS" to shift the decimal point positions (i.e. to read 100's of MHz instead of 10's of MHz, etc., as when the NORMAL input is used).

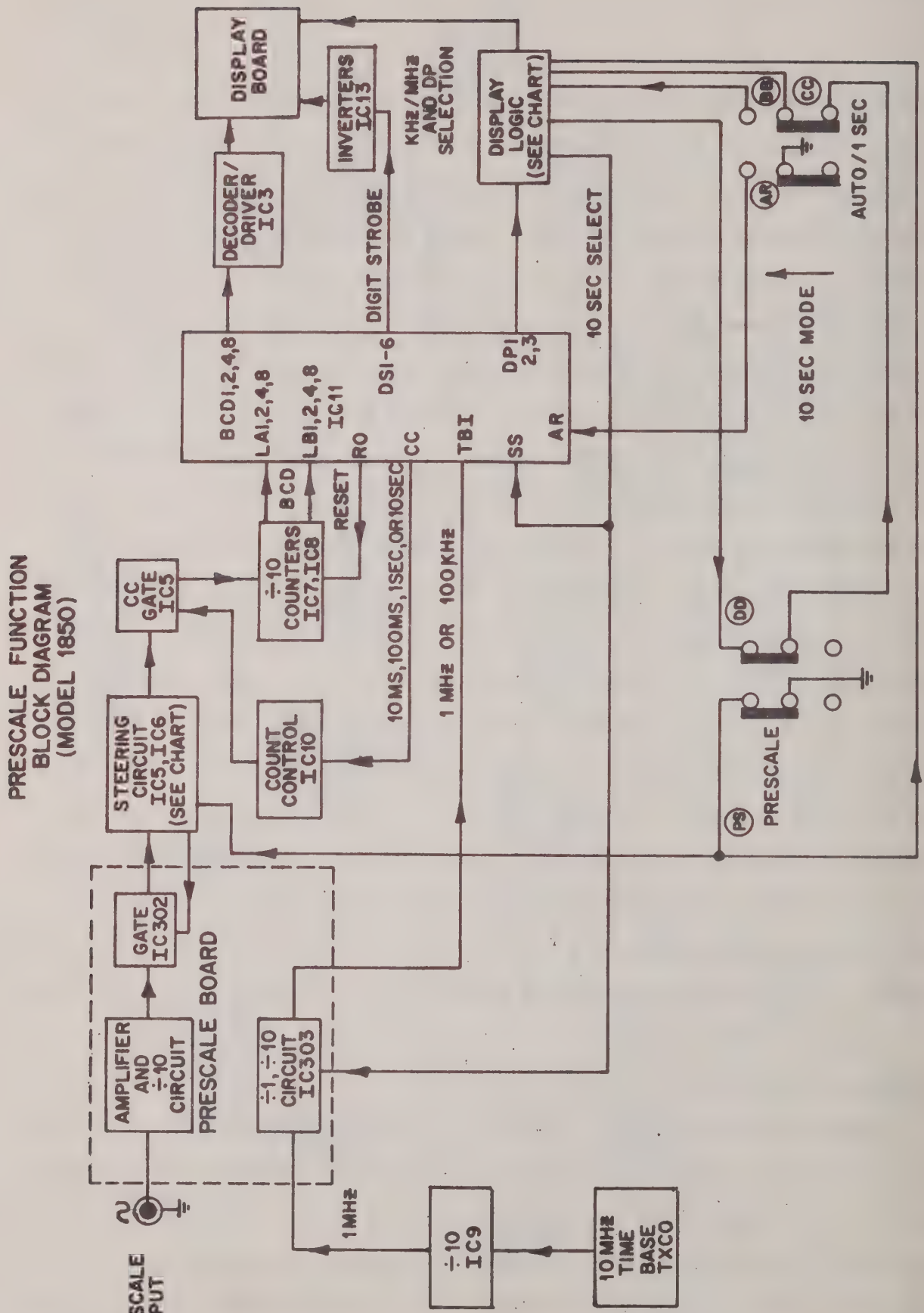

PRESCALE FUNCTION
BLOCK DIAGRAM
(MODEL 1850)
PRESCALE INPUT
PRESCALE BOARD
AMPLIFIER AND ÷10 CIRCUIT
GATE IC302
÷1, ÷10 CIRCUIT IC303
STEERING CIRCUIT IC5, IC6 (SEE CHART)
CC GATE IC5
COUNT CONTROL IC10
÷10 COUNTERS IC7, IC8
BCD
RESET
10MS, 100MS, 1SEC, OR 10SEC
1 MHz OR 100KHz
1MHz
÷10 IC9
10 MHz TIME BASE TXCO
BCD1,2,4,8
LA1,2,4,8
LB1,2,4,8
IC11
RO
CC
TBI
SS
AR
DSI-6
DP1 2,3
DIGIT STROBE
10 SEC SELECT
DECODER/ DRIVER IC3
INVERTERS IC13
DISPLAY BOARD
KHz/MHz AND DP SELECTION
DISPLAY LOGIC (SEE CHART)
10 SEC MODE
AUTO/1 SEC
PRESCALE
PS
DD
AR
BB
CC

FIG. 10

See Display Logic Chart, page 23.

The PRE-SCALER function operates the same as the FREQ function, except that an additional 10 second count control gate signal is used when the AUTO/1 SEC switch is placed in the 1 SEC (in) position. Since the input signal is divided-by-ten on the pre-scale PCB, 520MHz is "seen" as 52MHz by the counter section and 10MHz is seen as 1MHz. A 10 second count control is therefore needed in order to count frequency to the nearest Hz (52MHz x 10 sec = 520,000,000 cycles). A timebase divide-by-ten circuit is provided on the prescale PCB for the purpose of generating a 10 second "CC" gate signal. This is accomplished by driving the time base input, TBI (pin 15), of IC11 with a 100KHz instead of 1MHz signal, thus generating a 10 second instead of 1 second "CC" (pin 26) gate output. Since all the outputs of IC11 would be running at one-tenth normal speed in the 10 second mode, the digit strobes, DS1-DS6, and BCD outputs, BCD 1,2,4, and 8 must be brought back to normal speed to prevent flickering of the display digits. This is done internally by IC11 when the "SS" (pin 14) input is pulled low. Note that "SS" is pulled low at the same time the "TBI" input is changed to 100KHZ.

The input to the pre-scale PCB is terminated into 50Ω. The resistor network consisting of R313, 314, and 315 is necessary to match the 75Ω input impedance of the ATF417 high frequency hybrid amplifier (IC304) with the 50Ω impedance desired for the pre-scale input. See fig. 3B. The output of IC304 is AC coupled (internal capacitor) through R309 to the ECL high speed divide-by-ten device, IC301 (11C90). It is necessary to have approximately 350mV P-P signal at the input (pins 15 and 16) of IC301 for proper operation to 520MHz. Also, this input should have a ECL dc bias of approximately 3.5 V. The divide-by-ten output of IC301 is at TTL levels (pin 11). This drives the nand gate, 74LS00, IC302, pin 2. Pin 1 of IC302 is controlled by the function switching and goes "high" to enable this gate when the PRE-SCALE function is selected. The signal from pin 3 of IC302 is the "IP" input to the steering circuit as shown on the Steering Circuit Chart, page 5. R307 and R310 are load

resistors required for proper operation of the ECL outputs of IC301.

DISPLAY SECTION (Fig. 1F)

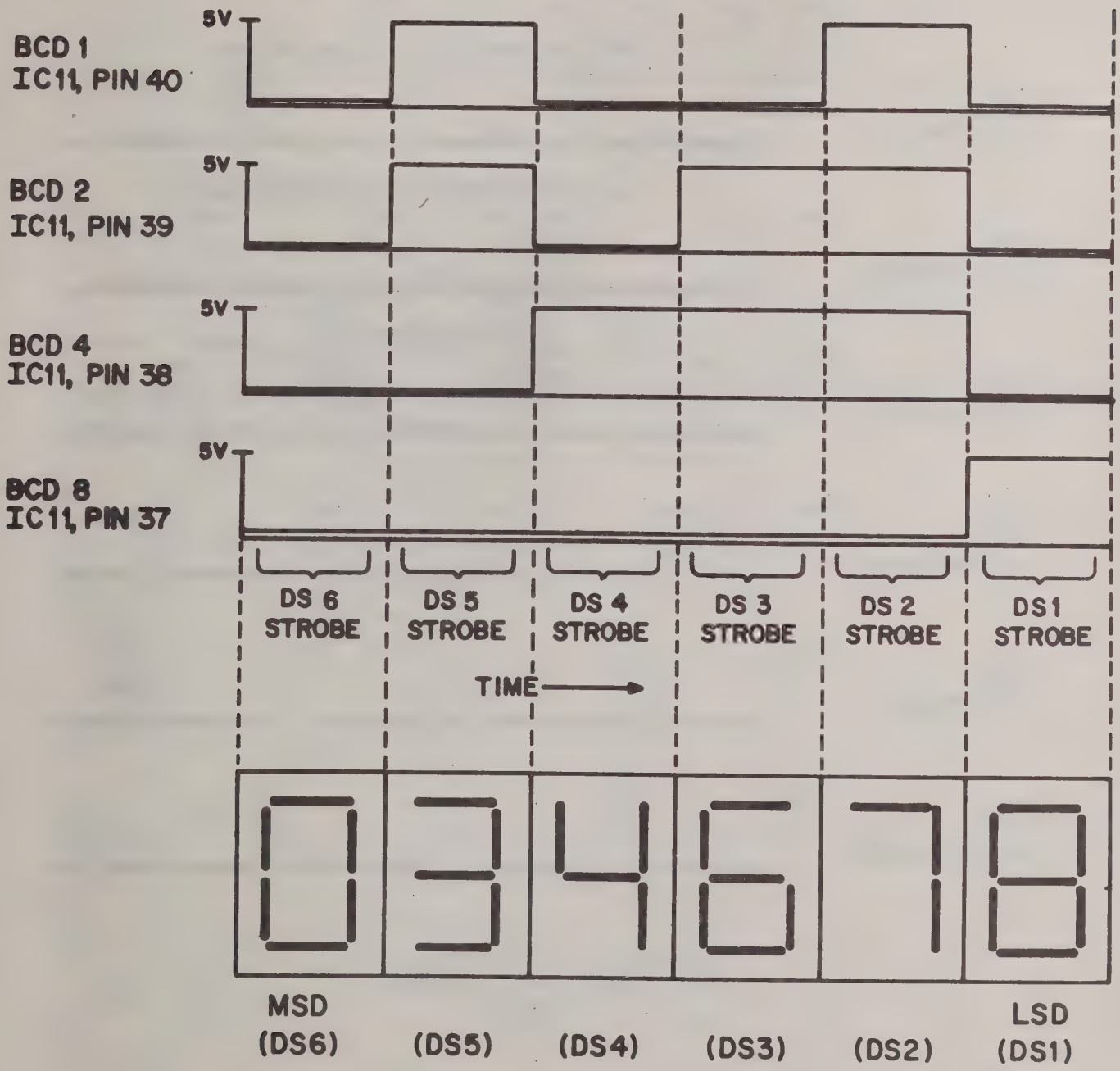
The BCD1, 2, 4, 8 and DS1-DS6 outputs of IC11 are multiplexed. The BCD outputs (pins 37-40) are decoded by IC3 into seven segment outputs that sink, in parallel, the digits DS101 through DS106, current limited by resistors R108-R114. DS1 through DS6 (pins 31-36) are strobed outputs that are inverted and buffered by IC13 to turn on transistors Q101 - Q106 and drive the digit displays. See waveforms Fig. 11 & Fig. 12. The leading zero blanking output, RBO (pin 3) of IC11 "signals" to IC 13 which zero digit is to be blanked. The logic for this blanking signal is internal to IC11 and cannot be changed. Note that proper blanking can be seen in the FREQ function with no input signal (the (3) most significant digits are blanked) and in the ACCU function (Model 1820) when pushing the RESET button (all digits, except the least significant digit, are blanked). The DP1, 2 and 3 outputs go "high", one at a time, depending upon the "CC" time base generated (see Frequency Function). Depending upon the function selected, the appropriate decimal point and KHz/us - MHz/ms indicators must turn on. For ease of trouble shooting the display logic circuit and knowing when a certain indicator is or isn't lit, the Display Logic Chart, page 23, is given for convenience. Also, the PCB Functional Layout chart, page 5, shows all the jumpers and different ICs required for proper operation of the main PCB. Refer to Parts Location, Main PCB, for jumper and IC locations. The overrange indicator, OVER, is driven by the inverter, pins 1, 2 of IC21, and controlled by the $\overline{OR}$ output (pin 30) of IC11. This output becomes active (pulses at a 10Hz rate in FREQ mode) when the display range has been exceeded.

POWER SUPPLY (Fig. 1G and Fig. 3C, 3D)

The power supply consists of a universal transformer, 50 or 60Hz, that can be wire-jumpered for either 120V or 240V operation. The power switch uses

EXAMPLE:

BCD 1, 2, 4 AND 8 OUTPUTS CORRESPONDING TO NUMERICAL FIGURES DISPLAYED.

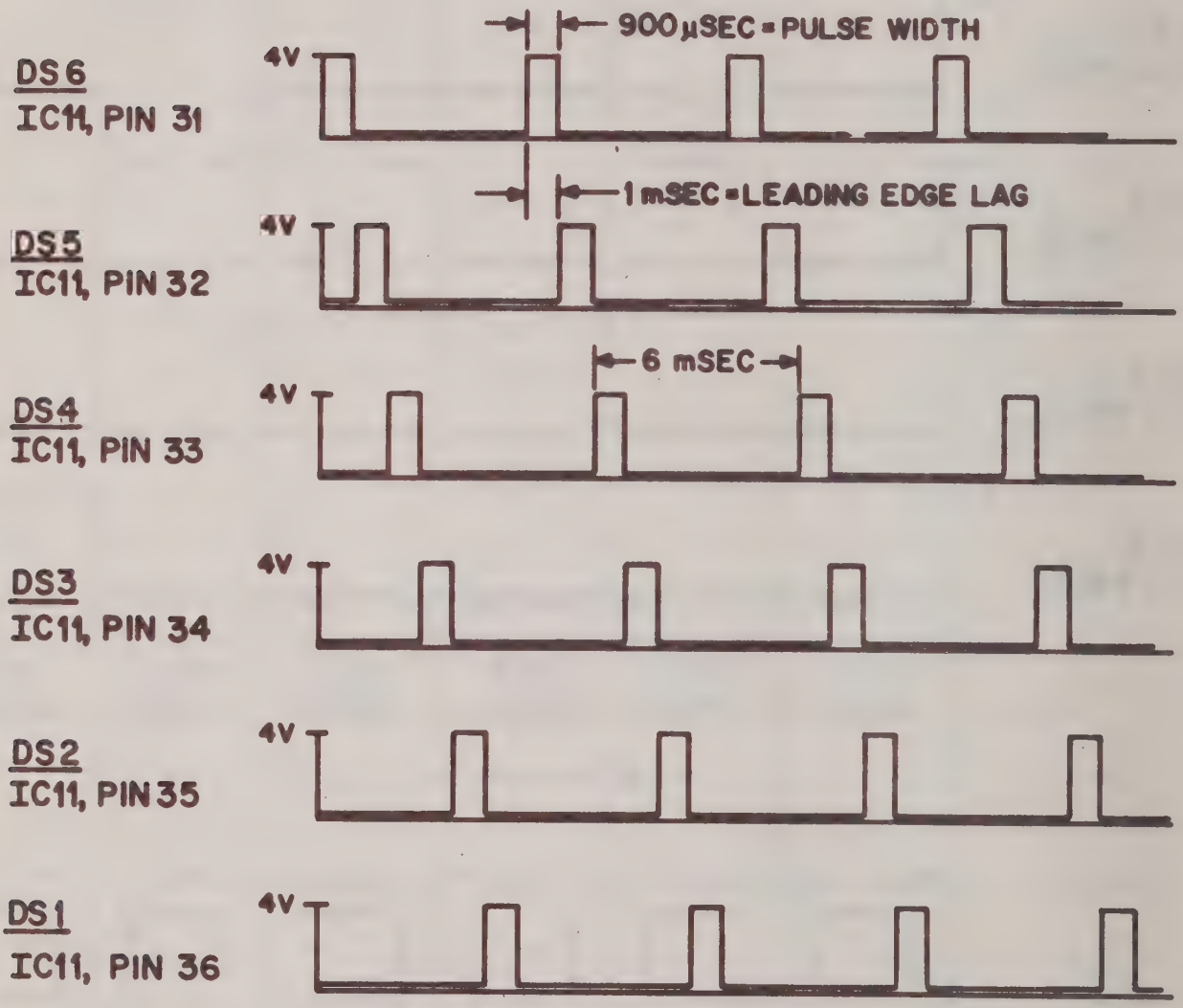


EXAMPLE OF BCD MULTIPLEXED DISPLAY

FIG. 11

NOTE:

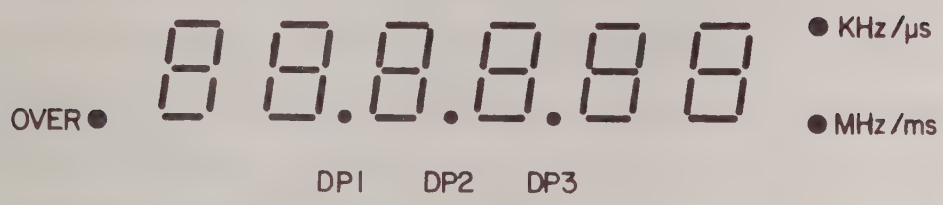
DS6 IS THE MOST SIGNIFICANT DIGIT (MSD) AND
DS1 IS THE LEAST SIGNIFICANT DIGIT (LSD).



STROBE SEQUENCE
FIG. 12

DISPLAY LOGIC CHART (Decimal Points, KHz/μs , MHz/ms and OVER Indicators)

Chart refers to the following L.E.D. display indicators;



and the following symbol definitions:

H = Logic "High" State
L = Logic "Low" State
X = Indicator Lit

Model	Function	AUTO / 1 SEC Switch Setting	Incoming Frequency	IC 11 DP Output			Display Indicator Lit					
				Pin 24 (10ms)	Pin 22 (100ms)	Pin 23 (1sec)	OVER	DP1	DP2	DP3	KHz/μs	MHz/ms
1802 1820 and 1850	FREQ	AUTO	<1MHz	L	L	H			X		X	
			>1MHz <10 MHz	L	H	L				X	X	
			>10MHz	H	L	L		X				X
		1 SEC	<1MHz	L	L	H			X		X	
			>1MHz	L	L	H	X		X		X	
	PERIOD	AUTO	<100Hz	H	L	L		X				X
			>100Hz <1KHz	L	H	L				X	X	
			>1KHz	L	L	H			X		X	
		1 SEC (100 Period Avg.)	>1KHz	L	L	H			X		X	
			<1KHz	L	L	H	X		X		X	
1820	ACCU	——	5Hz - 80MHz	L	L	H	**					
	TIME	——	——	L	L	H	**			X		
1850	PRESCALE	AUTO	<10MHz	L	L	H				X	X	
			>10MHz <100MHz	L	H	L		X				X
			>100MHz	H	L	L			X			X
		1 SEC (10 Sec)	10MHz - 520MHz	L	L	H	X		X		X	

** Lit only if display range of 999999 is exceeded.

secondary switching. The center tap is shorted to ground by the POWER switch to turn the unit on. The secondary has a dual winding for the +5 and +10 regulated voltages required. D1 and D2 and C1 full wave rectify and filter the +5 supply with an unregulated voltage of approximately 11 volts going into IC1, the +5 regulator. C3, a pin lead capacitor, is required to prevent the +5 regulator from going into oscillation. Note that a formed lead capacitor, instead of a pin lead for C3, may not stop IC1 from oscillating. D5 and D6 and C6 rectify and filter the +10 supply giving approximately 16 volts unregulated before going through the series limiting resistor R6 and zener regulator and capacitor, D7 and C7.

The model 1850 is also equipped for 11-16VDC external operation, with the addition of R1, R2 and D3, D4. Degredation of the input sensitivity specifications must be considered at 11V operation due to the lower +10 supply voltage on the main PCB which may be only 9 volts and the lower +20V supply on the Pre-scale PCB which may be only 18V in some cases. The POWER switch opens the circuit between the anodes of D3 and D4 and the 11-16 VDC external supply when the unit is turned off.

The Pre-scale PCB uses a DC-to-DC converter in order to generate the +20V supply required for operation of the ATF417 amplifier (IC 304). Note that this +20V supply is "sitting" on top of the +5V supply coming from the main PCB. The DC-to-DC converter therefore supplies from 16V to 19V (depending upon line voltage) on top of the +5V supply, giving 21 to 24 total volts with respect to ground at the cathodes of D301 and D302. C304 and C311 filter the supply before going through series resistor R306 and zener clamp D303.

Point "FF" on the Pre-scale PCB is the power input to the DC-to-DC converter. This voltage is the unregulated +5 supply voltage from the main PCB. R305 limits

the current input and C303 helps filter the supply voltage. Switching transistors, Q301 and Q302, in conjunction with R301 - 304, C301, 302 and transformer T301, provide the DC to DC conversion (oscillating at about 30KHz) with a current drain of approximately 130mA at 120V line operation.

SERVICE AND CALIBRATION

To service the unit, remove the rear case as follows:

1. Use a coin (a quarter works best) to remove the two screws that hold the handle to the case. Use caution to avoid losing the springs beneath the screws that hold the handle on the case. Remove handle
2. Remove the two Phillips head screws from the rear case.
3. Slide the rear case from the counter.
4. To re-install the rear case on the counter, follow the above procedure in reverse. When re-installing the rear case, be sure the printed circuit board(s) properly engage(s) the slots inside the case.

To calibrate the oscillator, a 10MHz standard with accuracy of at least ± 1 part in 10^8 is required to set the oscillator ± 1 Hz of 10MHz.

PROCEDURE:

1. Models 1802 and 1820 must be fully cased and warmed up for at least 1 hour before frequency adjustment is made (through hole provided in rear of case).
2. Model 1850 need not be warmed up and rear case must be removed (see Service, above).
3. Connect the standard frequency source to front panel NORMAL input.
4. Depress the FREQ and AUTO/ 1 SEC switches.

NOTE

The instrument will overrange and thus the MSDs will be lost.

5. For models 1802 and 1820, use a non-metallic alignment tool and

adjust C202 (right rear of the counter, on the vertical printed circuit board) through the hole in the rear case for a display equal to the standard frequency ±1 count.

6. For Model 1850, remove the seal screw on rear of TCXO (do not lose the rubber seal on the screw) and adjust slug with non-metallic alignment tool for reading of the standard frequency. Replace seal screw.

7. For Model 1850, re-assemble the rear case to the unit.

120V to 240V CONVERSION

The counter is factory-wired for use with 120V, 50/60 Hz AC lines. To operate the unit on 240V, 50/60 Hz, the internal connections must be changed. To convert the counter for 240 VAC operation, proceed as follows:

1. Remove the rear case of the counter as described in Service and Calibration.

2. Remove the jumper wire connecting holes L3 and L4 on the printed circuit board.

3. Remove the jumper wire connecting holes L2 and L5 on the p.c. board.

4. Connect a jumper wire between holes L4 and L5 on the p.c. board. This jumper may be placed on the component side or the bottom side of the circuit board: L4 and L5 are adjacent to each other.

5. Remove the 1/8-ampere (3/16-ampere, Model 1850) Type 3AG slo-blo fuse from the fuseholder at F1. Replace with 1/16-ampere (1/10-ampere, Model 1850) Type 3AG slo-blo fuse.

6. Make a notation of the change near the fuse label on the transformer bracket.

7. Re-assemble the rear case of the counter as described in Service and Calibration.

8. The wires within the detachable line cord are color-coded according to the European DIN standard. Connect the proper plug to match your outlet after the U.S. style plug has been removed.

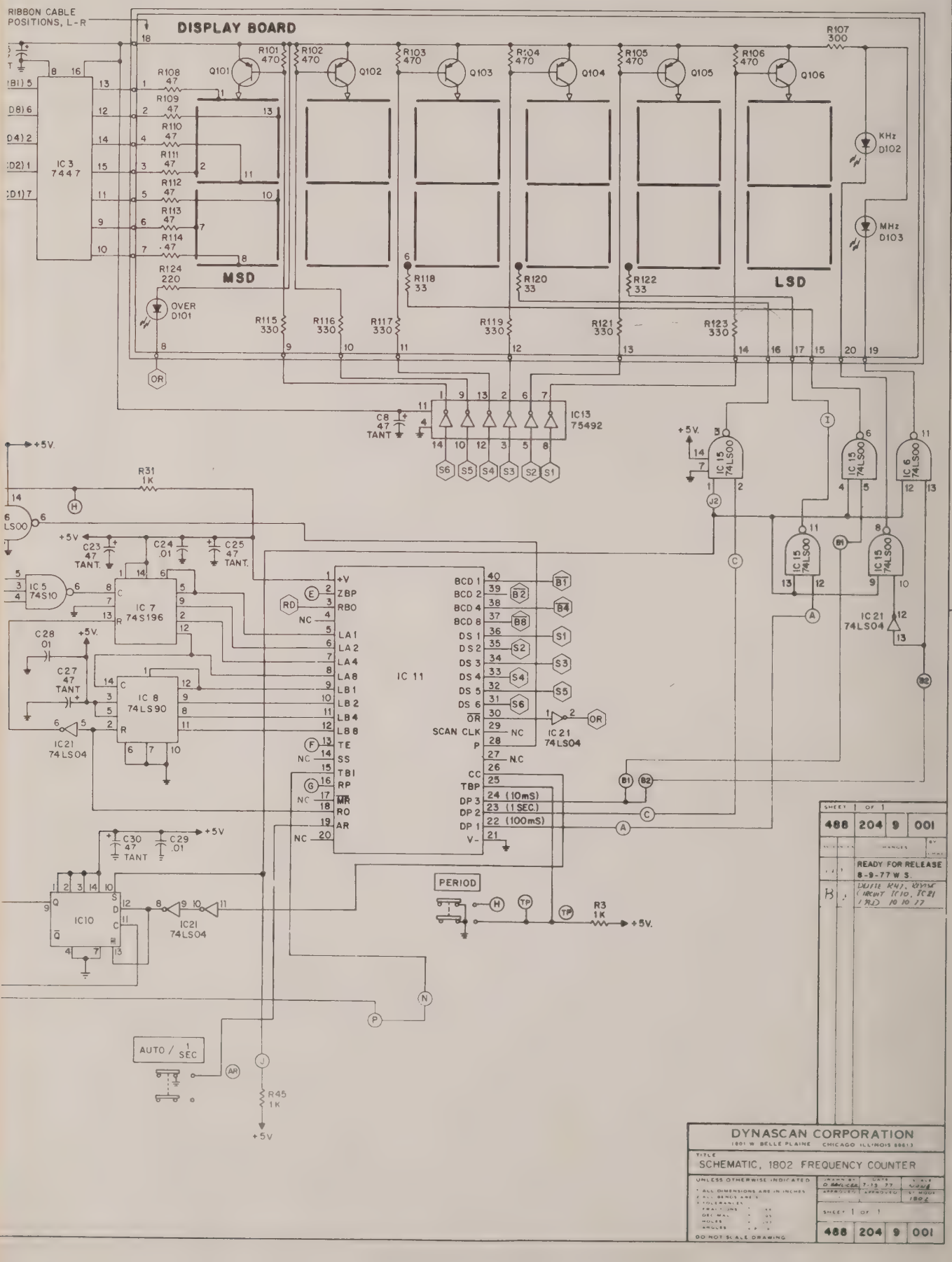
TCXO INSTALLATION

Refer to the Instruction Manual of each model for proper installation of its TCXO.

LAST NUMBER	NOT USED
R45, R124, R204	R1, R2, R5, R12, R13, R14, R15, R34, R35, R36, R37, R38, R39, R40, R41, R42
C31, C204	
D17, D103	D3, D4, D11, D12, D13, D14, D15, D16, D17
Q7, Q106, Q201	Q2, Q4, Q7
IC 21	IC2, IC 12, IC 14, IC 16, IC 17, IC 19, IC 20
J3	J1

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4W, 5%, DEPOSITED CARBON.
2. ALL CAPACITORS ARE SHOWN IN MICROFARADS
3. TITLES IN RECTANGLES DENOTE PANEL CONTROLS
4. FUNCTION SWITCHES SHOWN IN "FREQUENCY" MODE
5. IC 21 PIN 14 TO +5V., PIN 7 TO COMMON GROUND
6. ALL CIRCLES ◯ DENOTE PCB LETTERING
7. SYMBOLS —◯ ◯— INDICATE A PCB CONNECTION BETWEEN THESE POINTS.
8. SYMBOLS —◯— INDICATE A WIRE JUMPER ON PCB
9. ⬡ INDICATES AN UNMARKED PCB CONNECTION

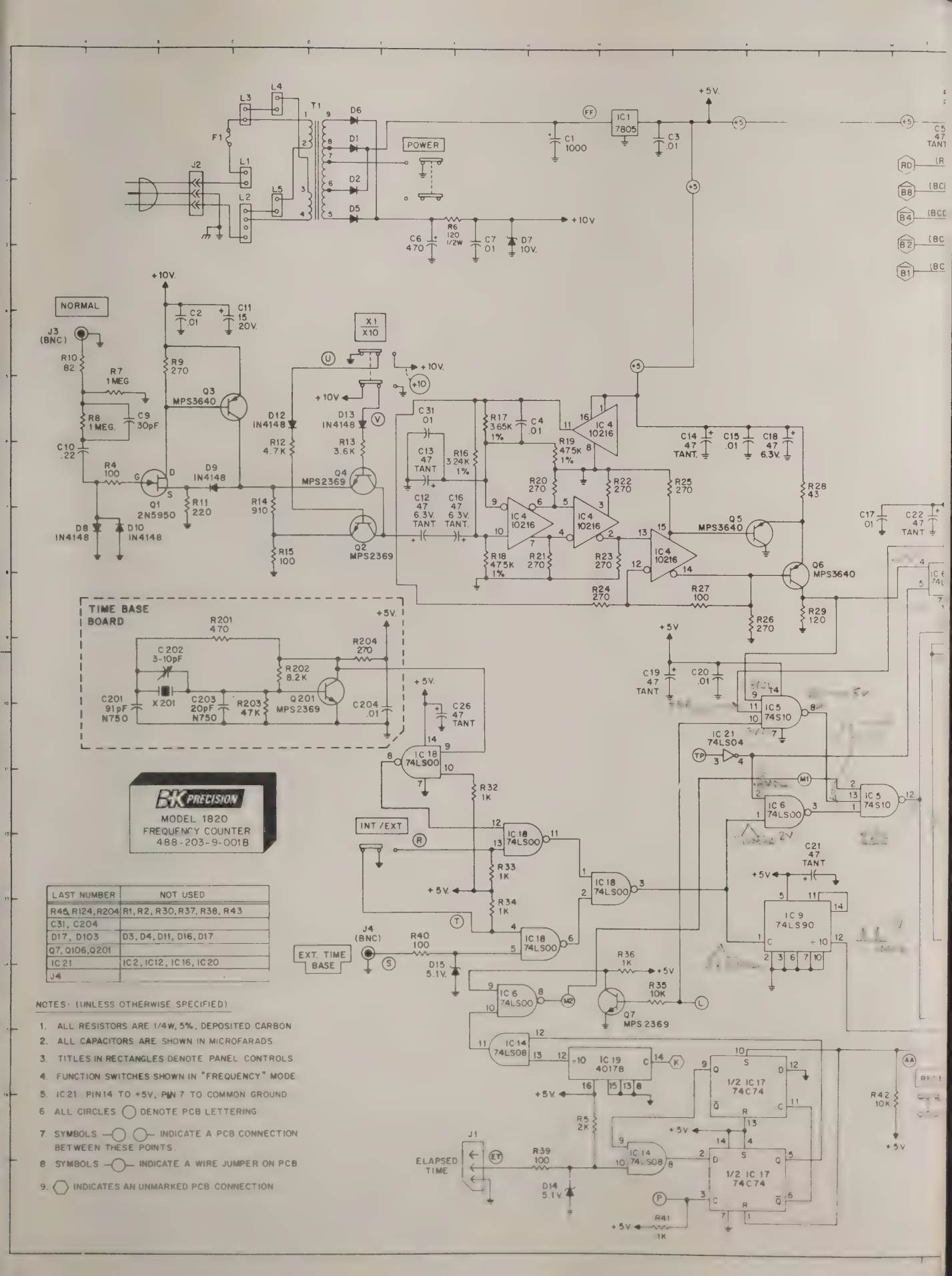


SHEET 1 OF 1			
488	204	9	001
REVISIONS			BY
READY FOR RELEASE 8-9-77 W.S.			
DELETE R43, R29 & INCRMT IC10, IC21 PER ECO 10-10-77			

DYNASCAN CORPORATION
1801 W. BELLE PLAINE CHICAGO ILLINOIS 60613

TITLE
SCHEMATIC, 1802 FREQUENCY COUNTER

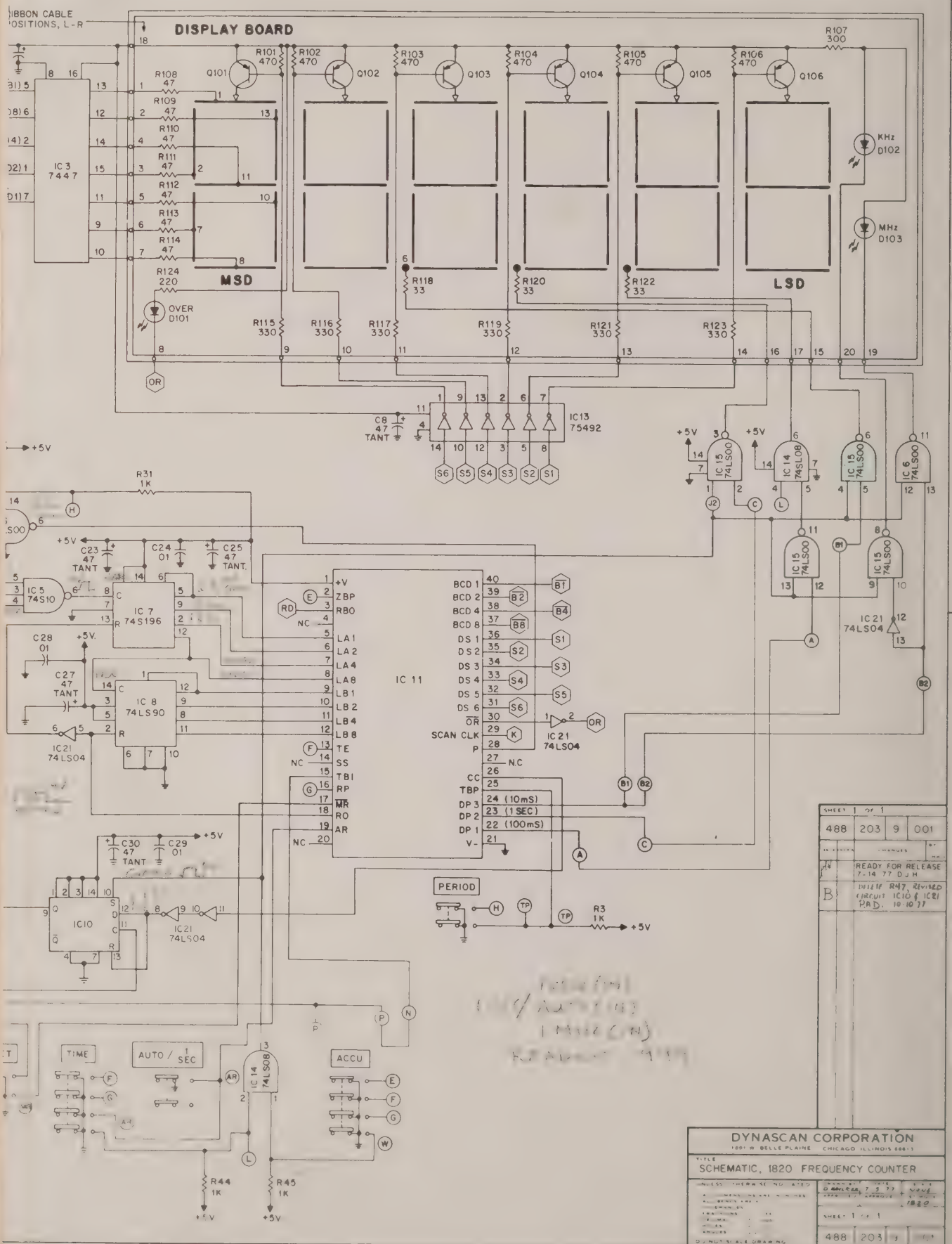
UNLESS OTHERWISE INDICATED	DRAWN BY O. RAMIREZ	DATE 7-13-77
* ALL DIMENSIONS ARE IN INCHES	APPROVED	APPROVED
* ALL DECIMALS ±		1802
* TOLERANCES FRACTIONS ± DEC MAL ± .03 ANGLES ± .5°	SHEET 1 OF 1	
DO NOT SCALE DRAWING	488 204 9 001	



LAST NUMBER	NOT USED
R45, R124, R204	R1, R2, R30, R37, R38, R43
C31, C204	
D17, D103	D3, D4, D11, D16, D17
Q7, Q106, Q201	
IC 21	IC 2, IC 12, IC 16, IC 20
J4	

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4W, 5%, DEPOSITED CARBON
2. ALL CAPACITORS ARE SHOWN IN MICROFARADS
3. TITLES IN RECTANGLES DENOTE PANEL CONTROLS
4. FUNCTION SWITCHES SHOWN IN "FREQUENCY" MODE
5. IC 21 PIN 14 TO +5V, PIN 7 TO COMMON GROUND
6. ALL CIRCLES ◯ DENOTE PCB LETTERING
7. SYMBOLS —◯ ◯— INDICATE A PCB CONNECTION BETWEEN THESE POINTS.
8. SYMBOLS —◯— INDICATE A WIRE JUMPER ON PCB
9. ⬡ INDICATES AN UNMARKED PCB CONNECTION

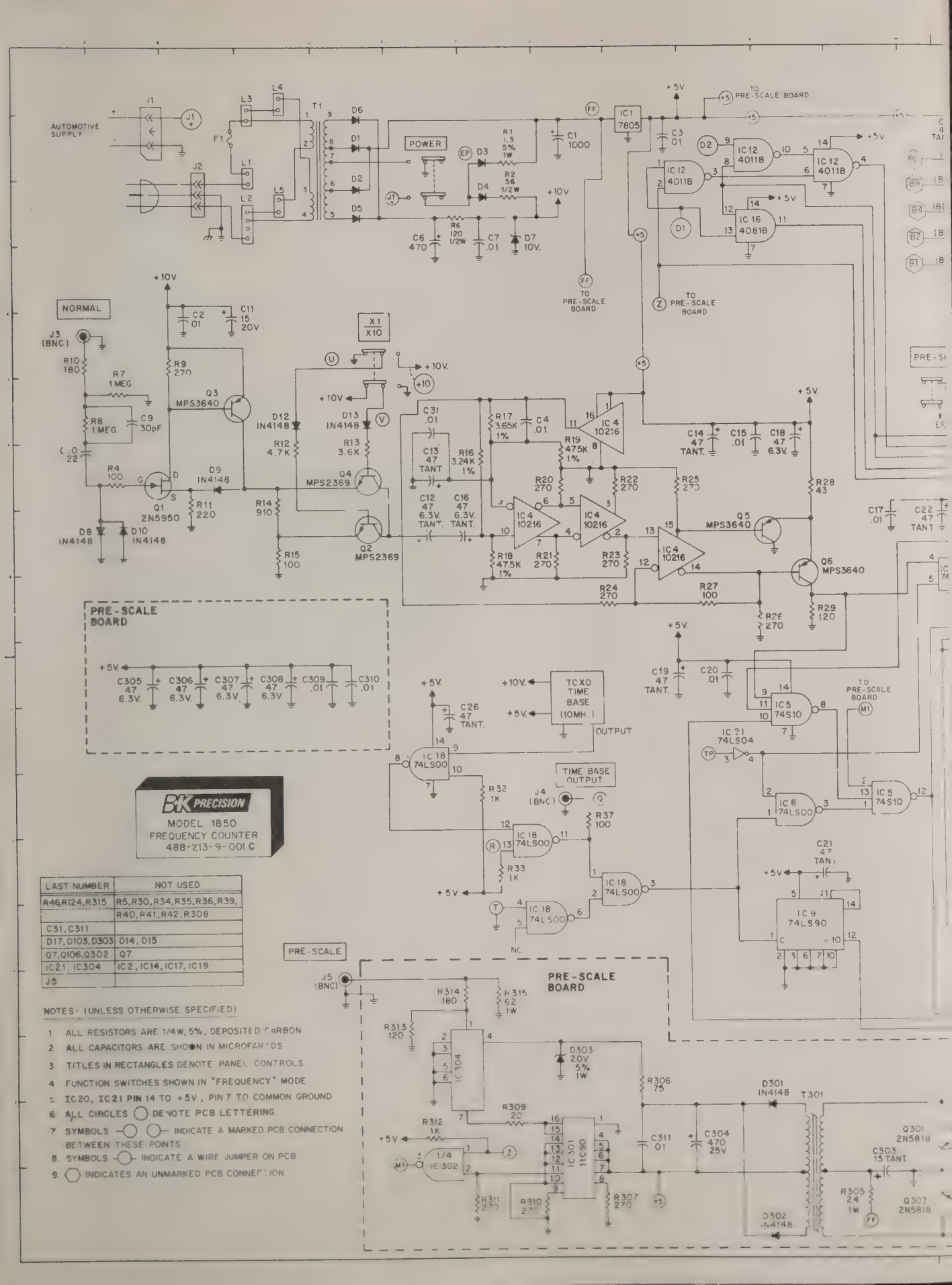


SHEET 1 OF 1			
488	203	9	001
	READY FOR RELEASE 7-14 77 D J M		
B	DELETE R47, REVISED CIRCUIT IC10 & IC21 PAD. 10-10-77		

DYNASCAN CORPORATION
1801 W. BELLE PLAINE CHICAGO, ILLINOIS 60613

TITLE
SCHEMATIC, 1820 FREQUENCY COUNTER

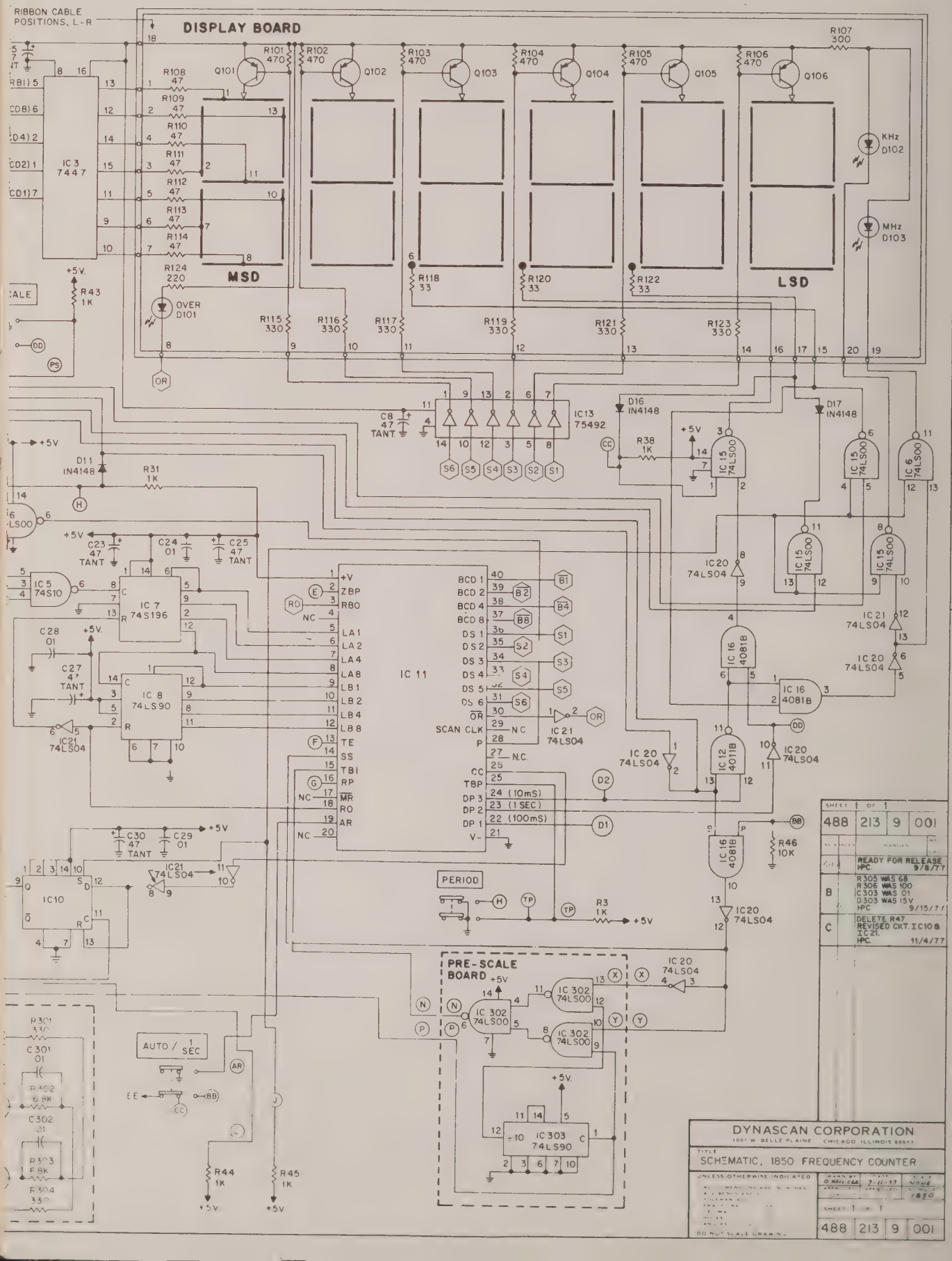
488	203	9	001



LAST NUMBER	NOT USED
R46,R124,R315	R5,R30,R34,R35,R36,R39, R40,R41,R42,R308
C31,C311	
D17,D103,D303	D14, D15
Q7,Q106,Q302	Q7
IC21, IC304	IC2, IC14, IC17, IC19
J5	

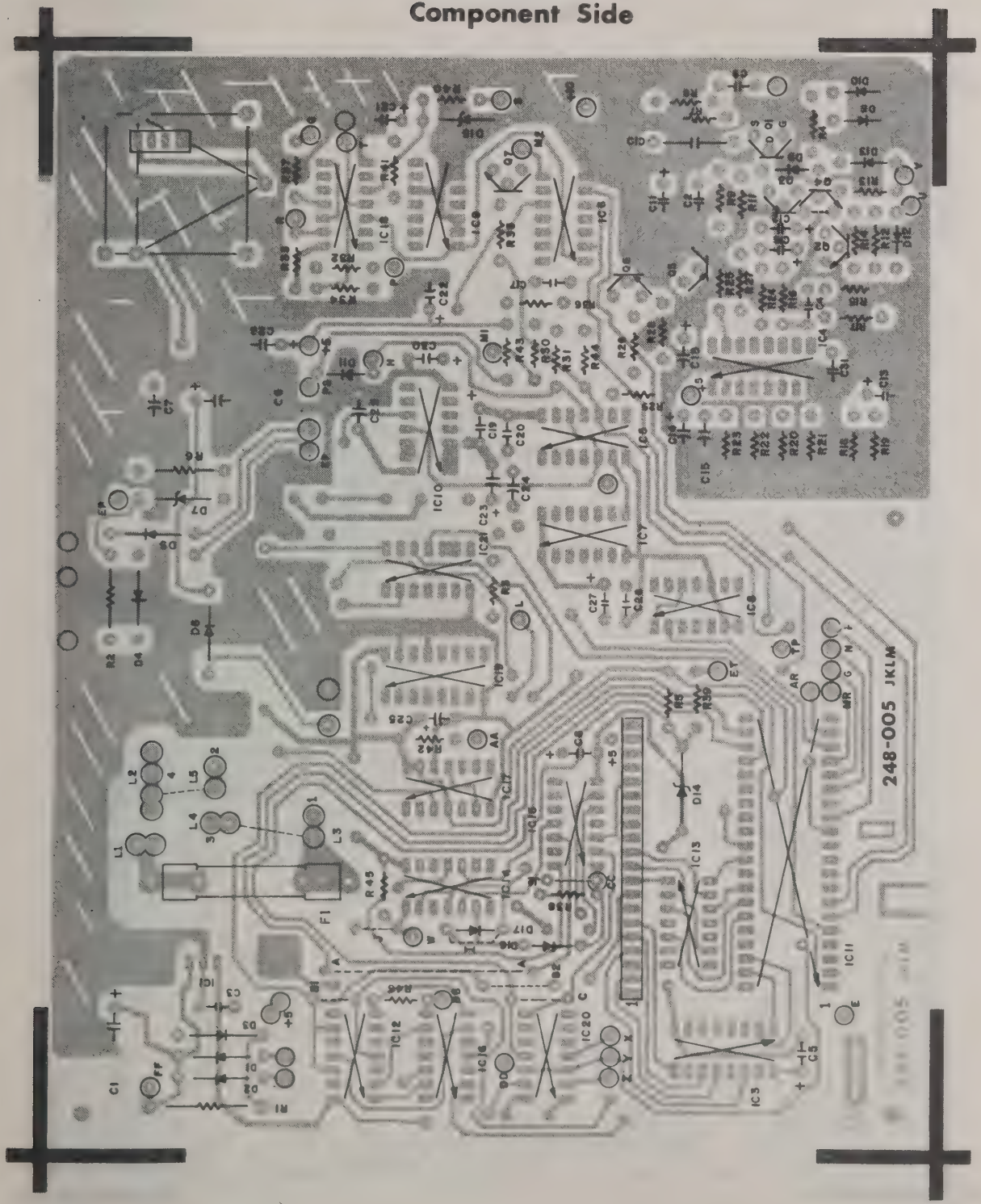
NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4W, 5%, DEPOSITED CARBON
2. ALL CAPACITORS ARE SHOWN IN MICROFARADS
3. TITLES IN RECTANGLES DENOTE PANEL CONTROLS
4. FUNCTION SWITCHES SHOWN IN "FREQUENCY" MODE
5. IC20, IC21 PIN 14 TO +5V., PIN 7 TO COMMON GROUND
6. ALL CIRCLES ◯ DENOTE PCB LETTERING.
7. SYMBOLS —◯ ◯— INDICATE A MARKED PCB CONNECTION BETWEEN THESE POINTS
8. SYMBOLS —◯— INDICATE A WIRE JUMPER ON PCB
9. ⬡ INDICATES AN UNMARKED PCB CONNECTION

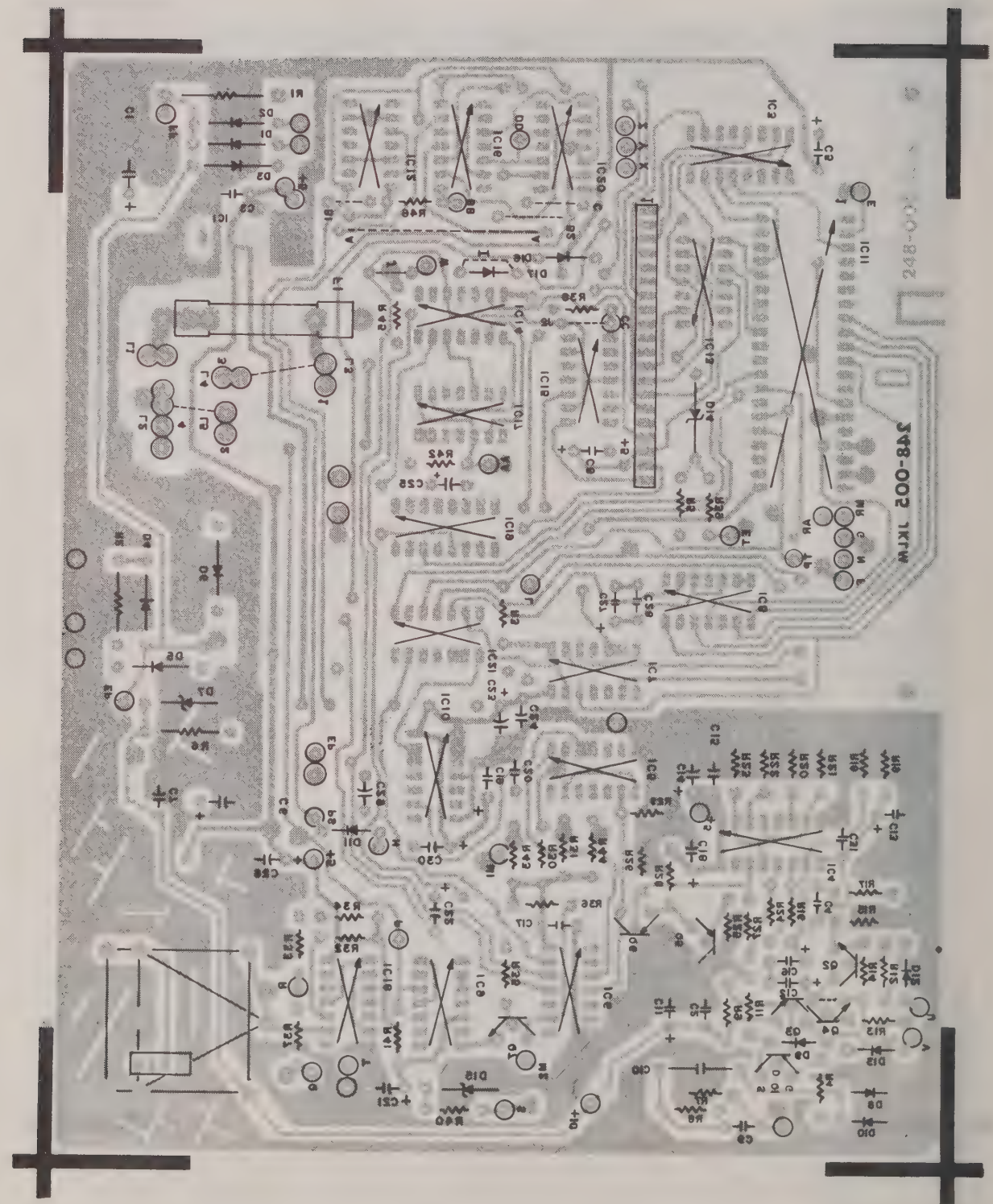

RIBBON CABLE POSITIONS, L-R
DISPLAY BOARD
MSD
LSD
IC 3 7447
Q101
Q102
Q103
Q104
Q105
Q106
KHz D102
MHz D103
OVER D101
IC 11
IC 7 74S196
IC 8 74LS90
IC 5 74S10
IC 13 75492
IC 10
PRE-SCALE BOARD
IC 302 74LS00
IC 303 74LS90
AUTO / 1 SEC
PERIOD
DYNASCAN CORPORATION
SCHEMATIC, 1850 FREQUENCY COUNTER
READY FOR RELEASE HPC. 9/8/77
R305 WAS 68
R306 WAS 100
C303 WAS 01
D303 WAS 15V
HPC 9/15/77
DELETE R47
REVISED CKT. IC10 & IC21.
HPC. 11/4/77
488 213 9 001

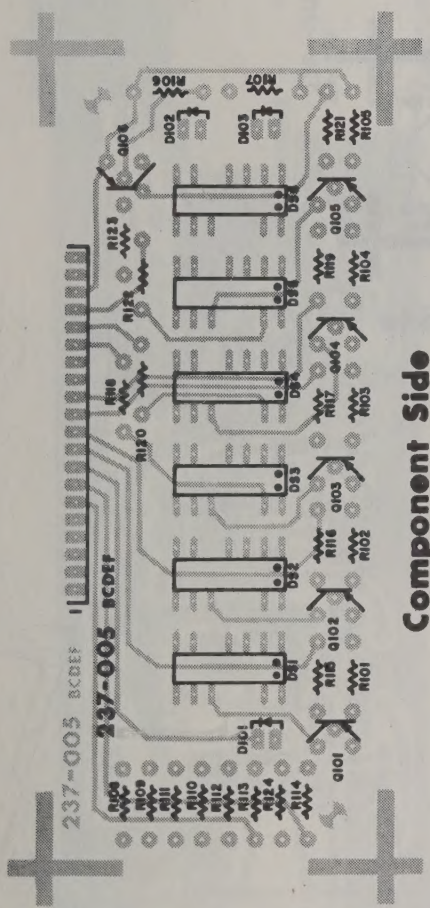
Main PCB

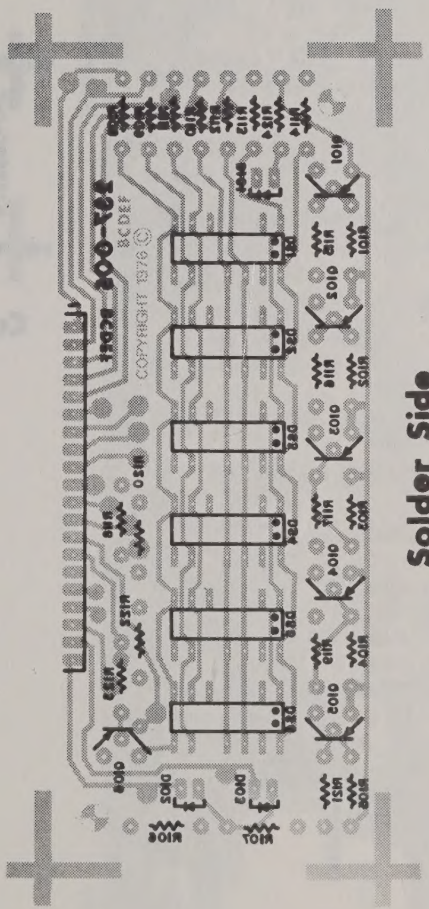
Component Side



Main PCB
Solder Side

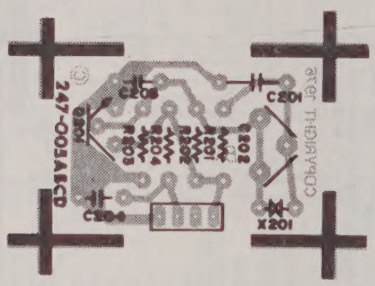



237-005 BCDEF
237-005 BCDEF
Component Side

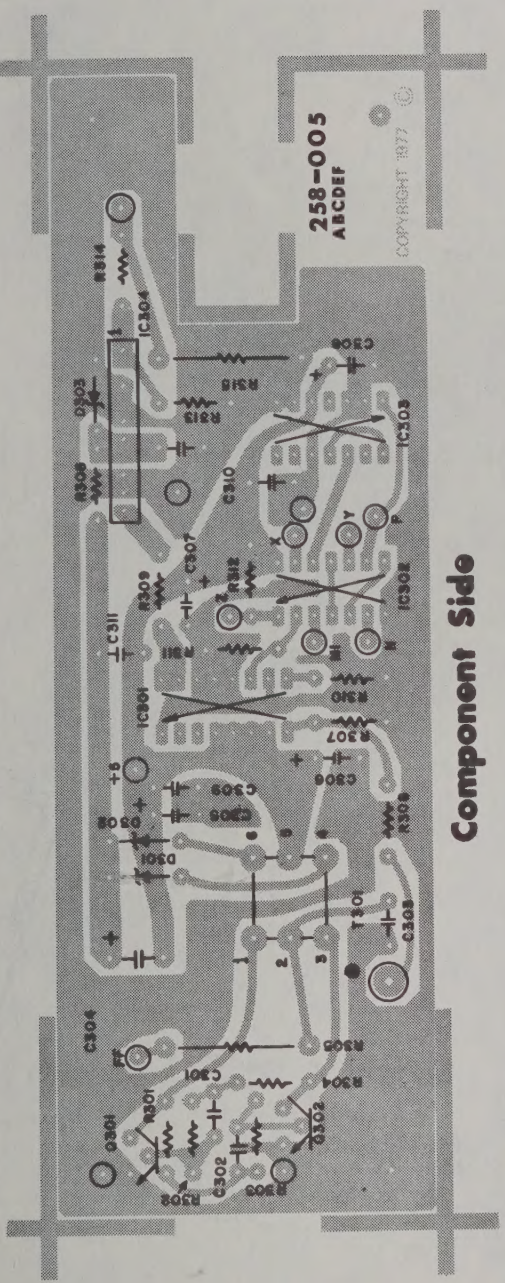

237-005 BCDEF
COPYRIGHT 1976
Solder Side

Display PCB

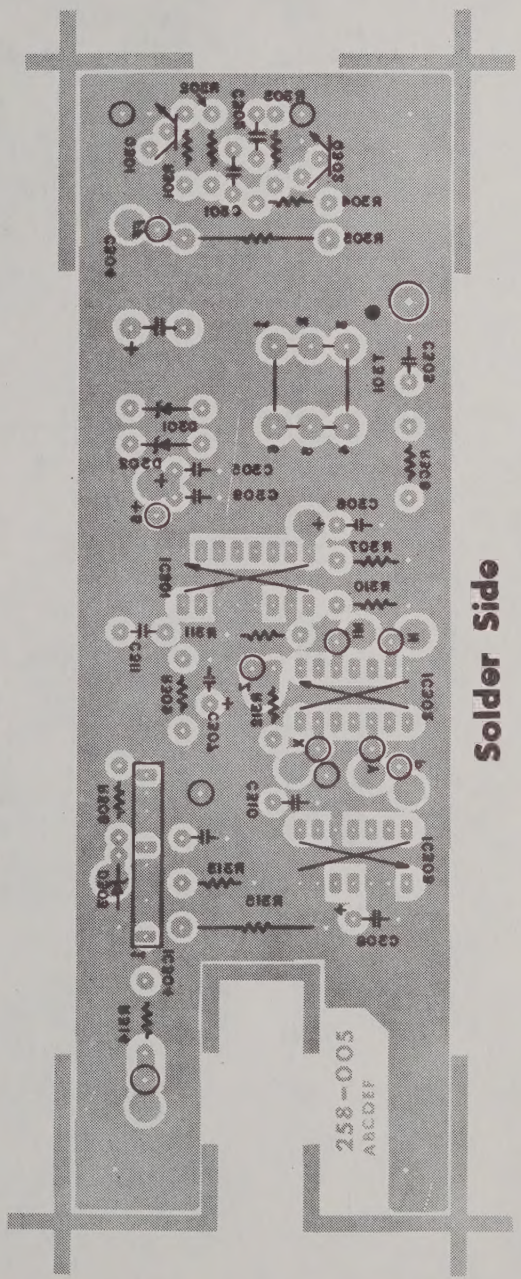
Time Base PCB



Component Side



Component Side



Solder Side

Prescale PCB